

## 2.4-GHz *Bluetooth*™ low energy and Proprietary System-on-Chip

Check for Samples: [CC2541](#)

### FEATURES

- **RF**
  - 2.4-GHz *Bluetooth* low energy Compliant and Proprietary RF System-on-Chip
  - Supports 250-kbps, 500-kbps, 1-Mbps, 2-Mbps Data Rates
  - Excellent Link Budget, Enabling Long-Range Applications Without External Front End
  - Programmable Output Power up to 0 dBm
  - Excellent Receiver Sensitivity (–94 dBm at 1 Mbps), Selectivity, and Blocking Performance
  - Suitable for Systems Targeting Compliance With Worldwide Radio Frequency Regulations: ETSI EN 300 328 and EN 300 440 Class 2 (Europe), FCC CFR47 Part 15 (US), and ARIB STD-T66 (Japan)
- **Layout**
  - Few External Components
  - Reference Design Provided
  - 6-mm × 6-mm QFN-40 Package
  - Pin-Compatible With CC2540 (When Not Using USB or I<sup>2</sup>C)
- **Low Power**
  - Active-Mode RX Down to: 17.9 mA
  - Active-Mode TX (0 dBm): 18.2 mA
  - Power Mode 1 (4-μs Wake-Up): 270 μA
  - Power Mode 2 (Sleep Timer On): 1 μA
  - Power Mode 3 (External Interrupts): 0.5 μA
  - Wide Supply-Voltage Range (2 V–3.6 V)
- **TPS62730 Compatible Low Power in Active Mode**
  - RX Down to: 14.7 mA (3-V supply)
  - TX (0 dBm): 14.3 mA (3-V supply)
- **High-Performance and Low-Power 8051 Microcontroller Core With Code Prefetch**
- **In-System-Programmable Flash, 128- or 256-KB**
- **8-KB RAM With Retention in All Power Modes**
- **Hardware Debug Support**
- **Extensive Baseband Automation, Including Auto-Acknowledgment and Address Decoding**
- **Retention of All Relevant Registers in All Power Modes**
- **Peripherals**
  - Powerful Five-Channel DMA
  - General-Purpose Timers (One 16-Bit, Two 8-Bit)
  - IR Generation Circuitry
  - 32-kHz Sleep Timer With Capture
  - Accurate Digital RSSI Support
  - Battery Monitor and Temperature Sensor
  - 12-Bit ADC With Eight Channels and Configurable Resolution
  - AES Security Coprocessor
  - Two Powerful USARTs With Support for Several Serial Protocols
  - 23 General-Purpose I/O Pins (21 × 4 mA, 2 × 20 mA)
  - I<sup>2</sup>C interface
  - 2 I/O Pins Have LED Driving Capabilities
  - Watchdog Timer
  - Integrated High-Performance Comparator
- **Development Tools**
  - CC2541 Evaluation Module Kit (CC2541EMK)
  - CC2541 Mini Development Kit (CC2541DK-MINI)
  - SmartRF™ Software
  - IAR Embedded Workbench™ Available
- **Microcontroller**



Please be aware that an important notice concerning availability, standard warranty, and use in critical applications of Texas Instruments semiconductor products and disclaimers thereto appears at the end of this data sheet.

Bluetooth is a trademark of Bluetooth SIG, Inc..

ZigBee is a registered trademark of ZigBee Alliance.

PRODUCTION DATA information is current as of publication date. Products conform to specifications per the terms of the Texas Instruments standard warranty. Production processing does not necessarily include testing of all parameters.

Copyright © 2012–2013, Texas Instruments Incorporated

## SOFTWARE FEATURES

- **Bluetooth v4.0 Compliant Protocol Stack for Single-Mode BLE Solution**
  - Complete Power-Optimized Stack, Including Controller and Host
    - GAP – Central, Peripheral, Observer, or Broadcaster (Including Combination Roles)
    - ATT / GATT – Client and Server
    - SMP – AES-128 Encryption and Decryption
    - L2CAP
  - Sample Applications and Profiles
    - Generic Applications for GAP Central and Peripheral Roles
    - Proximity, Accelerometer, Simple Keys, and Battery GATT Services
    - More Applications Supported in [BLE Software Stack](#)
  - Multiple Configuration Options
    - Single-Chip Configuration, Allowing Applications to Run on CC2541
    - Network Processor Interface for Applications Running on an External Microcontroller
  - BTool – Windows PC Application for Evaluation, Development, and Test

## APPLICATIONS

- 2.4-GHz *Bluetooth* low energy Systems
- Proprietary 2.4-GHz Systems
- Human-Interface Devices (Keyboard, Mouse, Remote Control)
- Sports and Leisure Equipment
- Mobile Phone Accessories
- Consumer Electronics

## CC2541 WITH [TPS62730](#)

- [TPS62730](#) is a 2-MHz Step-Down Converter With Bypass Mode
- Extends Battery Lifetime by up to 20%
- Reduced Current in All Active Modes
- 30-nA Bypass Mode Current to Support Low-Power Modes
- RF Performance Unchanged
- Small Package Allows for Small Solution Size
- CC2541 Controllable

## DESCRIPTION

The CC2541 is a power-optimized true system-on-chip (SoC) solution for both *Bluetooth* low energy and proprietary 2.4-GHz applications. It enables robust network nodes to be built with low total bill-of-material costs. The CC2541 combines the excellent performance of a leading RF transceiver with an industry-standard enhanced 8051 MCU, in-system programmable flash memory, 8-KB RAM, and many other powerful supporting features and peripherals. The CC2541 is highly suited for systems where ultralow power consumption is required. This is specified by various operating modes. Short transition times between operating modes further enable low power consumption.

The CC2541 is pin-compatible with the CC2540 in the 6-mm × 6-mm QFN40 package, if the USB is not used on the CC2540 and the I<sup>2</sup>C/extra I/O is not used on the CC2541. Compared to the CC2540, the CC2541 provides lower RF current consumption. The CC2541 does not have the USB interface of the CC2540, and provides lower maximum output power in TX mode. The CC2541 also adds a HW I<sup>2</sup>C interface.

The CC2541 is pin-compatible with the CC2533 RF4CE-optimized IEEE 802.15.4 SoC.

The CC2541 comes in two different versions: CC2541F128/F256, with 128 KB and 256 KB of flash memory, respectively.

For the CC2541 block diagram, see [Figure 1](#).



This integrated circuit can be damaged by ESD. Texas Instruments recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedures can cause damage.

ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because very small parametric changes could cause the device not to meet its published specifications.

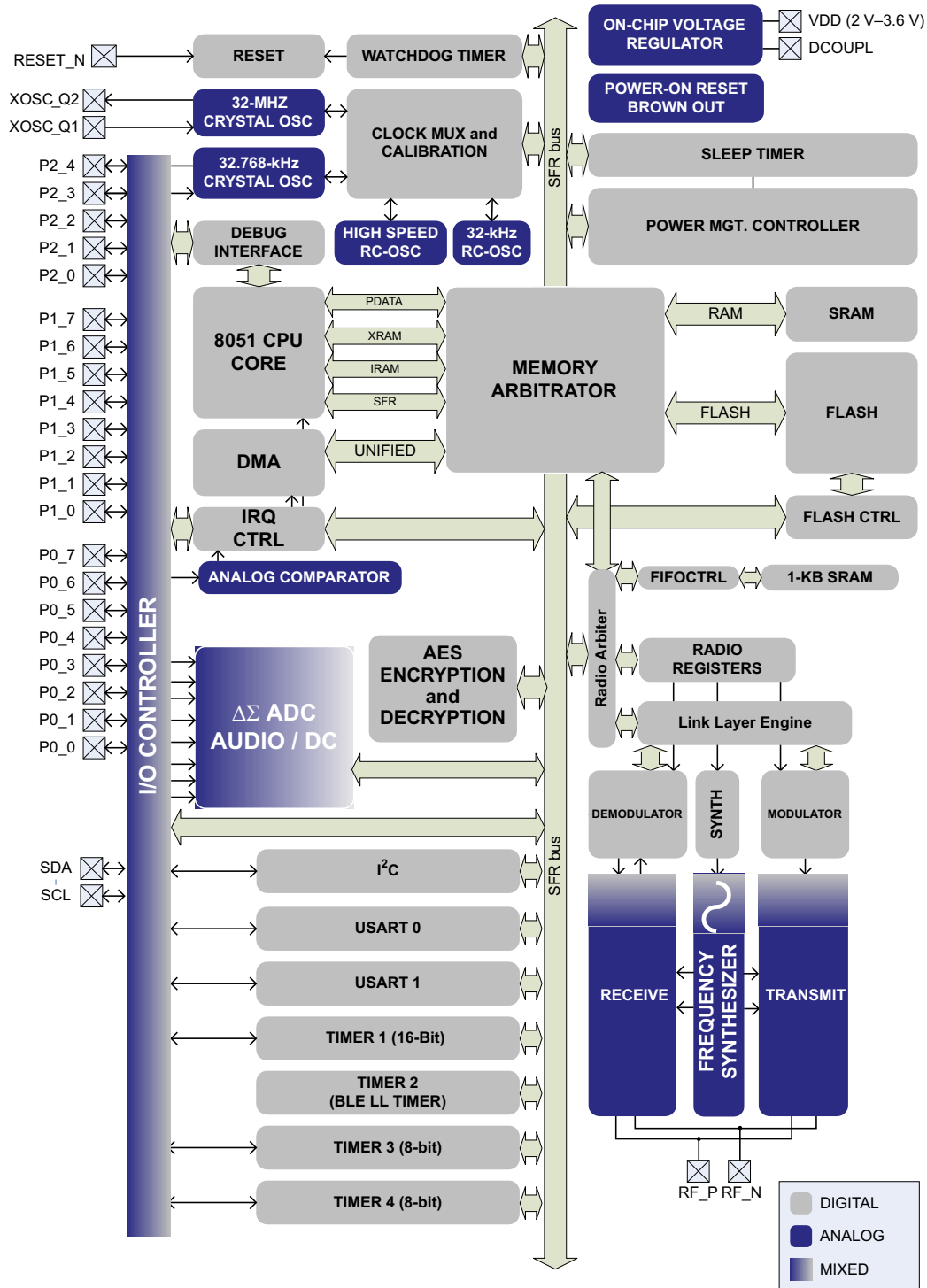


Figure 1. Block Diagram

## ABSOLUTE MAXIMUM RATINGS<sup>(1)</sup>

over operating free-air temperature range (unless otherwise noted)

|                            |                                                                                              | MIN  | MAX                     | UNIT |
|----------------------------|----------------------------------------------------------------------------------------------|------|-------------------------|------|
| Supply voltage             | All supply pins must have the same voltage                                                   | −0.3 | 3.9                     | V    |
| Voltage on any digital pin |                                                                                              | −0.3 | $V_{DD} + 0.3 \leq 3.9$ | V    |
| Input RF level             |                                                                                              |      | 10                      | dBm  |
| Storage temperature range  |                                                                                              | −40  | 125                     | °C   |
| ESD <sup>(2)</sup>         | All pins, excluding pins 25 and 26, according to human-body model, JEDEC STD 22, method A114 |      | 2                       | kV   |
|                            | All pins, according to human-body model, JEDEC STD 22, method A114                           |      | 1                       | kV   |
|                            | According to charged-device model, JEDEC STD 22, method C101                                 |      | 500                     | V    |

- (1) Stresses beyond those listed under *Absolute Maximum Ratings* may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under *Recommended Operating Conditions* is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
- (2) **CAUTION:** ESD sensitive device. Precautions should be used when handling the device in order to prevent permanent damage.

## RECOMMENDED OPERATING CONDITIONS

over operating free-air temperature range (unless otherwise noted)

|                                            | MIN | NOM | MAX | UNIT |
|--------------------------------------------|-----|-----|-----|------|
| Operating ambient temperature range, $T_A$ | −40 |     | 85  | °C   |
| Operating supply voltage                   | 2   |     | 3.6 | V    |

## ELECTRICAL CHARACTERISTICS

Measured on Texas Instruments CC2541 EM reference design with  $T_A = 25^\circ\text{C}$  and  $V_{DD} = 3\text{ V}$ ,  
**1 Mbps, GFSK, 250-kHz deviation, Bluetooth low energy mode, and 0.1% BER**

| PARAMETER                                                                                                         | TEST CONDITIONS                                                                                                                                                  | MIN | TYP  | MAX | UNIT          |
|-------------------------------------------------------------------------------------------------------------------|------------------------------------------------------------------------------------------------------------------------------------------------------------------|-----|------|-----|---------------|
| $I_{core}$ Core current consumption                                                                               | RX mode, standard mode, no peripherals active, low MCU activity                                                                                                  |     | 17.9 |     | mA            |
|                                                                                                                   | RX mode, high-gain mode, no peripherals active, low MCU activity                                                                                                 |     | 20.2 |     |               |
|                                                                                                                   | TX mode, −20 dBm output power, no peripherals active, low MCU activity                                                                                           |     | 16.8 |     |               |
|                                                                                                                   | TX mode, 0 dBm output power, no peripherals active, low MCU activity                                                                                             |     | 18.2 |     |               |
|                                                                                                                   | Power mode 1. Digital regulator on; 16-MHz RCOSC and 32-MHz crystal oscillator off; 32.768-kHz XOSC, POR, BOD and sleep timer active; RAM and register retention |     | 270  |     | $\mu\text{A}$ |
|                                                                                                                   | Power mode 2. Digital regulator off; 16-MHz RCOSC and 32-MHz crystal oscillator off; 32.768-kHz XOSC, POR, and sleep timer active; RAM and register retention    |     | 1    |     |               |
|                                                                                                                   | Power mode 3. Digital regulator off; no clocks; POR active; RAM and register retention                                                                           |     | 0.5  |     |               |
|                                                                                                                   | Low MCU activity: 32-MHz XOSC running. No radio or peripherals. Limited flash access, no RAM access.                                                             |     | 6.7  |     | mA            |
| $I_{peri}$ Peripheral current consumption<br>(Adds to core current $I_{core}$ for each peripheral unit activated) | Timer 1. Timer running, 32-MHz XOSC used                                                                                                                         |     | 90   |     | $\mu\text{A}$ |
|                                                                                                                   | Timer 2. Timer running, 32-MHz XOSC used                                                                                                                         |     | 90   |     |               |
|                                                                                                                   | Timer 3. Timer running, 32-MHz XOSC used                                                                                                                         |     | 60   |     |               |
|                                                                                                                   | Timer 4. Timer running, 32-MHz XOSC used                                                                                                                         |     | 70   |     |               |
|                                                                                                                   | Sleep timer, including 32.753-kHz RCOSC                                                                                                                          |     | 0.6  |     |               |
|                                                                                                                   | ADC, when converting                                                                                                                                             |     | 1.2  |     | mA            |

## GENERAL CHARACTERISTICS

Measured on Texas Instruments CC2541 EM reference design with  $T_A = 25^\circ\text{C}$  and  $V_{DD} = 3\text{ V}$

| PARAMETER                       | TEST CONDITIONS                                                                                                                                                                                                 | MIN  | TYP | MAX  | UNIT |
|---------------------------------|-----------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|------|-----|------|------|
| WAKE-UP AND TIMING              |                                                                                                                                                                                                                 |      |     |      |      |
| Power mode 1 → Active           | Digital regulator on, 16-MHz RCOSC and 32-MHz crystal oscillator off. Start-up of 16-MHz RCOSC                                                                                                                  |      | 4   |      | μs   |
| Power mode 2 or 3 → Active      | Digital regulator off, 16-MHz RCOSC and 32-MHz crystal oscillator off. Start-up of regulator and 16-MHz RCOSC                                                                                                   |      | 120 |      | μs   |
| Active → TX or RX               | Crystal ESR = 16 Ω. Initially running on 16-MHz RCOSC, with 32-MHz XOSC OFF                                                                                                                                     |      | 500 |      | μs   |
|                                 | With 32-MHz XOSC initially on                                                                                                                                                                                   |      | 180 |      | μs   |
| RX/TX turnaround                | Proprietary auto mode                                                                                                                                                                                           |      | 130 |      | μs   |
|                                 | BLE mode                                                                                                                                                                                                        |      | 150 |      |      |
| RADIO PART                      |                                                                                                                                                                                                                 |      |     |      |      |
| RF frequency range              | Programmable in 1-MHz steps                                                                                                                                                                                     | 2379 |     | 2496 | MHz  |
| Data rate and modulation format | 2 Mbps, GFSK, 500-kHz deviation<br>2 Mbps, GFSK, 320-kHz deviation<br>1 Mbps, GFSK, 250-kHz deviation<br>1 Mbps, GFSK, 160-kHz deviation<br>500 kbps, MSK<br>250 kbps, GFSK, 160-kHz deviation<br>250 kbps, MSK |      |     |      |      |

## RF RECEIVE SECTION

Measured on Texas Instruments CC2541 EM reference design with  $T_A = 25^\circ\text{C}$ ,  $V_{DD} = 3\text{ V}$ ,  $f_c = 2440\text{ MHz}$

| PARAMETER                                        | TEST CONDITIONS                                                                                         | MIN  | TYP | MAX | UNIT |
|--------------------------------------------------|---------------------------------------------------------------------------------------------------------|------|-----|-----|------|
| <b>2 Mbps, GFSK, 500-kHz Deviation, 0.1% BER</b> |                                                                                                         |      |     |     |      |
| Receiver sensitivity                             |                                                                                                         |      | –90 |     | dBm  |
| Saturation                                       | BER < 0.1%                                                                                              |      | –1  |     | dBm  |
| Co-channel rejection                             | Wanted signal at –67 dBm                                                                                |      | –9  |     | dB   |
| In-band blocking rejection                       | $\pm 2\text{ MHz}$ offset, 0.1% BER, wanted signal –67 dBm                                              |      | –2  |     | dB   |
|                                                  | $\pm 4\text{ MHz}$ offset, 0.1% BER, wanted signal –67 dBm                                              |      | 36  |     |      |
|                                                  | $\pm 6\text{ MHz}$ or greater offset, 0.1% BER, wanted signal –67 dBm                                   |      | 41  |     |      |
| Frequency error tolerance <sup>(1)</sup>         | Including both initial tolerance and drift. Sensitivity better than –67dBm, 250 byte payload. BER 0.1%  | –300 |     | 300 | kHz  |
| Symbol rate error tolerance <sup>(2)</sup>       | Maximum packet length. Sensitivity better than –67dBm, 250 byte payload. BER 0.1%                       | –120 |     | 120 | ppm  |
| <b>2 Mbps, GFSK, 320-kHz Deviation, 0.1% BER</b> |                                                                                                         |      |     |     |      |
| Receiver sensitivity                             |                                                                                                         |      | –86 |     | dBm  |
| Saturation                                       | BER < 0.1%                                                                                              |      | –7  |     | dBm  |
| Co-channel rejection                             | Wanted signal at –67 dBm                                                                                |      | –12 |     | dB   |
| In-band blocking rejection                       | $\pm 2\text{ MHz}$ offset, 0.1% BER, wanted signal –67 dBm                                              |      | –1  |     | dB   |
|                                                  | $\pm 4\text{ MHz}$ offset, 0.1% BER, wanted signal –67 dBm                                              |      | 34  |     |      |
|                                                  | $\pm 6\text{ MHz}$ or greater offset, 0.1% BER, wanted signal –67 dBm                                   |      | 39  |     |      |
| Frequency error tolerance <sup>(1)</sup>         | Including both initial tolerance and drift. Sensitivity better than –67 dBm, 250 byte payload. BER 0.1% | –300 |     | 300 | kHz  |
| Symbol rate error tolerance <sup>(2)</sup>       | Maximum packet length. Sensitivity better than –67 dBm, 250 byte payload. BER 0.1%                      | –120 |     | 120 | ppm  |

(1) Difference between center frequency of the received RF signal and local oscillator frequency

(2) Difference between incoming symbol rate and the internally generated symbol rate

## RF RECEIVE SECTION (continued)

Measured on Texas Instruments CC2541 EM reference design with  $T_A = 25^\circ\text{C}$ ,  $V_{DD} = 3\text{ V}$ ,  $f_c = 2440\text{ MHz}$

| PARAMETER                                                                   | TEST CONDITIONS                                                                                         | MIN  | TYP | MAX | UNIT |
|-----------------------------------------------------------------------------|---------------------------------------------------------------------------------------------------------|------|-----|-----|------|
| <b>1 Mbps, GFSK, 250-kHz Deviation, Bluetooth low energy Mode, 0.1% BER</b> |                                                                                                         |      |     |     |      |
| Receiver sensitivity <sup>(3)(4)</sup>                                      | High-gain mode                                                                                          |      | –94 |     | dBm  |
|                                                                             | Standard mode                                                                                           |      | –88 |     |      |
| Saturation <sup>(4)</sup>                                                   | BER < 0.1%                                                                                              |      | 5   |     | dBm  |
| Co-channel rejection <sup>(4)</sup>                                         | Wanted signal –67 dBm                                                                                   |      | –6  |     | dB   |
| In-band blocking rejection <sup>(4)</sup>                                   | ±1 MHz offset, 0.1% BER, wanted signal –67 dBm                                                          |      | –2  |     | dB   |
|                                                                             | ±2 MHz offset, 0.1% BER, wanted signal –67 dBm                                                          |      | 26  |     |      |
|                                                                             | ±3 MHz offset, 0.1% BER, wanted signal –67 dBm                                                          |      | 34  |     |      |
|                                                                             | >6 MHz offset, 0.1% BER, wanted signal –67 dBm                                                          |      | 33  |     |      |
| Out-of-band blocking rejection <sup>(4)</sup>                               | Minimum interferer level < 2 GHz (Wanted signal –67 dBm)                                                |      | –21 |     | dBm  |
|                                                                             | Minimum interferer level [2 GHz, 3 GHz] (Wanted signal –67 dBm)                                         |      | –25 |     |      |
|                                                                             | Minimum interferer level > 3 GHz (Wanted signal –67 dBm)                                                |      | –7  |     |      |
| Intermodulation <sup>(4)</sup>                                              | Minimum interferer level                                                                                |      | –36 |     | dBm  |
| Frequency error tolerance <sup>(5)</sup>                                    | Including both initial tolerance and drift. Sensitivity better than –67dBm, 250 byte payload. BER 0.1%  | –250 |     | 250 | kHz  |
| Symbol rate error tolerance <sup>(6)</sup>                                  | Maximum packet length. Sensitivity better than –67 dBm, 250 byte payload. BER 0.1%                      | –80  |     | 80  | ppm  |
| <b>1 Mbps, GFSK, 160-kHz Deviation, 0.1% BER</b>                            |                                                                                                         |      |     |     |      |
| Receiver sensitivity <sup>(7)</sup>                                         |                                                                                                         |      | –91 |     | dBm  |
| Saturation                                                                  | BER < 0.1%                                                                                              |      | 0   |     | dBm  |
| Co-channel rejection                                                        | Wanted signal 10 dB above sensitivity level                                                             |      | –9  |     | dB   |
| In-band blocking rejection                                                  | ±1-MHz offset, 0.1% BER, wanted signal –67 dBm                                                          |      | 2   |     | dB   |
|                                                                             | ±2-MHz offset, 0.1% BER, wanted signal –67 dBm                                                          |      | 24  |     |      |
|                                                                             | ±3-MHz offset, 0.1% BER, wanted signal –67 dBm                                                          |      | 27  |     |      |
|                                                                             | >6-MHz offset, 0.1% BER, wanted signal –67 dBm                                                          |      | 32  |     |      |
| Frequency error tolerance <sup>(5)</sup>                                    | Including both initial tolerance and drift. Sensitivity better than –67 dBm, 250-byte payload. BER 0.1% | –200 |     | 200 | kHz  |
| Symbol rate error tolerance <sup>(6)</sup>                                  | Maximum packet length. Sensitivity better than –67 dBm, 250-byte payload. BER 0.1%                      | –80  |     | 80  | ppm  |
| <b>500 kbps, MSK, 0.1% BER</b>                                              |                                                                                                         |      |     |     |      |
| Receiver sensitivity <sup>(7)</sup>                                         |                                                                                                         |      | –99 |     | dBm  |
| Saturation                                                                  | BER < 0.1%                                                                                              |      | 0   |     | dBm  |
| Co-channel rejection                                                        | Wanted signal –67 dBm                                                                                   |      | –5  |     | dB   |
| In-band blocking rejection                                                  | ±1-MHz offset, 0.1% BER, wanted signal –67 dBm                                                          |      | 20  |     | dB   |
|                                                                             | ±2-MHz offset, 0.1% BER, wanted signal –67 dBm                                                          |      | 27  |     |      |
|                                                                             | >2-MHz offset, 0.1% BER, wanted signal –67 dBm                                                          |      | 28  |     |      |
| Frequency error tolerance                                                   | Including both initial tolerance and drift. Sensitivity better than –67 dBm, 250-byte payload. BER 0.1% | –150 |     | 150 | kHz  |
| Symbol rate error tolerance                                                 | Maximum packet length. Sensitivity better than –67 dBm, 250-byte payload. BER 0.1%                      | –80  |     | 80  | ppm  |

(3) The receiver sensitivity setting is programmable using a TI BLE stack vendor-specific API command. The default value is standard mode.

(4) Results based on standard-gain mode.

(5) Difference between center frequency of the received RF signal and local oscillator frequency

(6) Difference between incoming symbol rate and the internally generated symbol rate

(7) Results based on high-gain mode.

## RF RECEIVE SECTION (continued)

Measured on Texas Instruments CC2541 EM reference design with  $T_A = 25^\circ\text{C}$ ,  $V_{DD} = 3\text{ V}$ ,  $f_c = 2440\text{ MHz}$

| PARAMETER                                          | TEST CONDITIONS                                                                                         | MIN  | TYP | MAX | UNIT |
|----------------------------------------------------|---------------------------------------------------------------------------------------------------------|------|-----|-----|------|
| <b>250 kbps, GFSK, 160 kHz Deviation, 0.1% BER</b> |                                                                                                         |      |     |     |      |
| Receiver sensitivity <sup>(8)</sup>                |                                                                                                         |      | –98 |     | dBm  |
| Saturation                                         | BER < 0.1%                                                                                              |      | 0   |     | dBm  |
| Co-channel rejection                               | Wanted signal –67 dBm                                                                                   |      | –3  |     | dB   |
| In-band blocking rejection                         | ±1-MHz offset, 0.1% BER, wanted signal –67 dBm                                                          |      | 23  |     | dB   |
|                                                    | ±2-MHz offset, 0.1% BER, wanted signal –67 dBm                                                          |      | 28  |     |      |
|                                                    | >2-MHz offset, 0.1% BER, wanted signal –67 dBm                                                          |      | 29  |     |      |
| Frequency error tolerance <sup>(9)</sup>           | Including both initial tolerance and drift. Sensitivity better than –67 dBm, 250-byte payload. BER 0.1% | –150 |     | 150 | kHz  |
| Symbol rate error tolerance <sup>(10)</sup>        | Maximum packet length. Sensitivity better than –67 dBm, 250-byte payload. BER 0.1%                      | –80  |     | 80  | ppm  |
| <b>250 kbps, MSK, 0.1% BER</b>                     |                                                                                                         |      |     |     |      |
| Receiver sensitivity <sup>(11)</sup>               |                                                                                                         |      | –99 |     | dBm  |
| Saturation                                         | BER < 0.1%                                                                                              |      | 0   |     | dBm  |
| Co-channel rejection                               | Wanted signal –67 dBm                                                                                   |      | –5  |     | dB   |
| In-band blocking rejection                         | ±1-MHz offset, 0.1% BER, wanted signal –67 dBm                                                          |      | 20  |     | dB   |
|                                                    | ±2-MHz offset, 0.1% BER, wanted signal –67 dBm                                                          |      | 29  |     |      |
|                                                    | >2-MHz offset, 0.1% BER, wanted signal –67 dBm                                                          |      | 30  |     |      |
| Frequency error tolerance                          | Including both initial tolerance and drift. Sensitivity better than –67 dBm, 250-byte payload. BER 0.1% | –150 |     | 150 | kHz  |
| Symbol rate error tolerance                        | Maximum packet length. Sensitivity better than –67 dBm, 250-byte payload. BER 0.1%                      | –80  |     | 80  | ppm  |
| <b>ALL RATES/FORMATS</b>                           |                                                                                                         |      |     |     |      |
| Spurious emission in RX. Conducted measurement     | $f < 1\text{ GHz}$                                                                                      |      | –67 |     | dBm  |
| Spurious emission in RX. Conducted measurement     | $f > 1\text{ GHz}$                                                                                      |      | –57 |     | dBm  |

(8) Results based on standard-gain mode.

(9) Difference between center frequency of the received RF signal and local oscillator frequency

(10) Difference between incoming symbol rate and the internally generated symbol rate

(11) Results based on high-gain mode.

## RF TRANSMIT SECTION

Measured on Texas Instruments CC2541 EM reference design with  $T_A = 25^\circ\text{C}$ ,  $V_{DD} = 3\text{ V}$  and  $f_c = 2440\text{ MHz}$

| PARAMETER                               | TEST CONDITIONS                                                                                                                                                                        | MIN | TYP     | MAX | UNIT |
|-----------------------------------------|----------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|-----|---------|-----|------|
| Output power                            | Delivered to a single-ended 50-Ω load through a balun using maximum recommended output power setting                                                                                   |     | 0       |     | dBm  |
|                                         | Delivered to a single-ended 50-Ω load through a balun using minimum recommended output power setting                                                                                   |     | –23     |     |      |
| Programmable output power range         | Delivered to a single-ended 50-Ω load through a balun using minimum recommended output power setting                                                                                   |     | 23      |     | dB   |
| Spurious emission conducted measurement | $f < 1\text{ GHz}$                                                                                                                                                                     |     | –52     |     | dBm  |
|                                         | $f > 1\text{ GHz}$                                                                                                                                                                     |     | –48     |     | dBm  |
|                                         | Suitable for systems targeting compliance with worldwide radio-frequency regulations ETSI EN 300 328 and EN 300 440 Class 2 (Europe), FCC CFR47 Part 15 (US), and ARIB STD-T66 (Japan) |     |         |     |      |
| Optimum load impedance                  | Differential impedance as seen from the RF port (RF_P and RF_N) toward the antenna                                                                                                     |     | 70 +j30 |     | Ω    |

Designs with antenna connectors that require conducted ETSI compliance at 64 MHz should insert an LC resonator in front of the antenna connector. Use a 1.6-nH inductor in parallel with a 1.8-pF capacitor. Connect both from the signal trace to a good RF ground.

## CURRENT CONSUMPTION WITH TPS62730

Measured on Texas Instruments CC2541 TPA62730 EM reference design with  $T_A = 25^\circ\text{C}$ ,  $V_{DD} = 3\text{ V}$  and  $f_c = 2440\text{ MHz}$ , **1 Mbps, GFSK, 250-kHz deviation, Bluetooth™ low energy Mode, 1% BER<sup>(1)</sup>**

| PARAMETER           | TEST CONDITIONS                                                                      | MIN | TYP  | MAX | UNIT |
|---------------------|--------------------------------------------------------------------------------------|-----|------|-----|------|
| Current consumption | RX mode, standard mode, no peripherals active, low MCU activity, MCU at 1 MHz        |     | 14.7 |     | mA   |
|                     | RX mode, high-gain mode, no peripherals active, low MCU activity, MCU at 1 MHz       |     | 16.7 |     |      |
|                     | TX mode, –20 dBm output power, no peripherals active, low MCU activity, MCU at 1 MHz |     | 13.1 |     |      |
|                     | TX mode, 0 dBm output power, no peripherals active, low MCU activity, MCU at 1 MHz   |     | 14.3 |     |      |

(1) 0.1% BER maps to 30.8% PER

## 32-MHz CRYSTAL OSCILLATOR

Measured on Texas Instruments CC2541 EM reference design with  $T_A = 25^\circ\text{C}$  and  $V_{DD} = 3\text{ V}$

| PARAMETER                                             | TEST CONDITIONS                                                                                                                                                                                                      | MIN | TYP  | MAX | UNIT |
|-------------------------------------------------------|----------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|-----|------|-----|------|
| Crystal frequency                                     |                                                                                                                                                                                                                      |     | 32   |     | MHz  |
| Crystal frequency accuracy requirement <sup>(1)</sup> |                                                                                                                                                                                                                      | –40 |      | 40  | ppm  |
| ESR Equivalent series resistance                      |                                                                                                                                                                                                                      | 6   |      | 60  | Ω    |
| $C_0$ Crystal shunt capacitance                       |                                                                                                                                                                                                                      | 1   |      | 7   | pF   |
| $C_L$ Crystal load capacitance                        |                                                                                                                                                                                                                      | 10  |      | 16  | pF   |
| Start-up time                                         |                                                                                                                                                                                                                      |     | 0.25 |     | ms   |
| Power-down guard time                                 | The crystal oscillator must be in power down for a guard time before it is used again. This requirement is valid for all modes of operation. The need for power-down guard time can vary with crystal type and load. | 3   |      |     | ms   |

(1) Including aging and temperature dependency, as specified by [1]

## 32.768-kHz CRYSTAL OSCILLATOR

 Measured on Texas Instruments CC2541 EM reference design with  $T_A = 25^\circ\text{C}$  and  $V_{DD} = 3\text{ V}$ 

| PARAMETER                                             | TEST CONDITIONS | MIN | TYP    | MAX | UNIT       |
|-------------------------------------------------------|-----------------|-----|--------|-----|------------|
| Crystal frequency                                     |                 |     | 32.768 |     | kHz        |
| Crystal frequency accuracy requirement <sup>(1)</sup> |                 | –40 |        | 40  | ppm        |
| ESR Equivalent series resistance                      |                 |     | 40     | 130 | k $\Omega$ |
| $C_0$ Crystal shunt capacitance                       |                 |     | 0.9    | 2   | pF         |
| $C_L$ Crystal load capacitance                        |                 |     | 12     | 16  | pF         |
| Start-up time                                         |                 |     | 0.4    |     | s          |

(1) Including aging and temperature dependency, as specified by [1]

## 32-kHz RC OSCILLATOR

 Measured on Texas Instruments CC2541 EM reference design with  $T_A = 25^\circ\text{C}$  and  $V_{DD} = 3\text{ V}$ .

| PARAMETER                                 | TEST CONDITIONS | MIN | TYP         | MAX | UNIT                |
|-------------------------------------------|-----------------|-----|-------------|-----|---------------------|
| Calibrated frequency <sup>(1)</sup>       |                 |     | 32.753      |     | kHz                 |
| Frequency accuracy after calibration      |                 |     | $\pm 0.2\%$ |     |                     |
| Temperature coefficient <sup>(2)</sup>    |                 |     | 0.4         |     | %/ $^\circ\text{C}$ |
| Supply-voltage coefficient <sup>(3)</sup> |                 |     | 3           |     | %/V                 |
| Calibration time <sup>(4)</sup>           |                 |     | 2           |     | ms                  |

(1) The calibrated 32-kHz RC oscillator frequency is the 32-MHz XTAL frequency divided by 977.

(2) Frequency drift when temperature changes after calibration

(3) Frequency drift when supply voltage changes after calibration

(4) When the 32-kHz RC oscillator is enabled, it is calibrated when a switch from the 16-MHz RC oscillator to the 32-MHz crystal oscillator is performed while SLEEP\_CMD.OSC32K\_CALDIS is set to 0.

## 16-MHz RC OSCILLATOR

 Measured on Texas Instruments CC2541 EM reference design with  $T_A = 25^\circ\text{C}$  and  $V_{DD} = 3\text{ V}$ 

| PARAMETER                               | TEST CONDITIONS | MIN | TYP         | MAX | UNIT          |
|-----------------------------------------|-----------------|-----|-------------|-----|---------------|
| Frequency <sup>(1)</sup>                |                 |     | 16          |     | MHz           |
| Uncalibrated frequency accuracy         |                 |     | $\pm 18\%$  |     |               |
| Calibrated frequency accuracy           |                 |     | $\pm 0.6\%$ |     |               |
| Start-up time                           |                 |     | 10          |     | $\mu\text{s}$ |
| Initial calibration time <sup>(2)</sup> |                 |     | 50          |     | $\mu\text{s}$ |

(1) The calibrated 16-MHz RC oscillator frequency is the 32-MHz XTAL frequency divided by 2.

(2) When the 16-MHz RC oscillator is enabled, it is calibrated when a switch from the 16-MHz RC oscillator to the 32-MHz crystal oscillator is performed while SLEEP\_CMD.OSC\_PD is set to 0.

## RSSI CHARACTERISTICS

Measured on Texas Instruments CC2541 EM reference design with  $T_A = 25^\circ\text{C}$  and  $V_{DD} = 3\text{ V}$

| PARAMETER                                                                                      | TEST CONDITIONS               | MIN | TYP     | MAX | UNIT |
|------------------------------------------------------------------------------------------------|-------------------------------|-----|---------|-----|------|
| <b>2 Mbps, GFSK, 320-kHz Deviation, 0.1% BER and 2 Mbps, GFSK, 500-kHz Deviation, 0.1% BER</b> |                               |     |         |     |      |
| Useful RSSI range <sup>(1)</sup>                                                               | Reduced gain by AGC algorithm |     | 64      |     | dB   |
|                                                                                                | High gain by AGC algorithm    |     | 64      |     |      |
| RSSI offset <sup>(1)</sup>                                                                     | Reduced gain by AGC algorithm |     | 79      |     | dBm  |
|                                                                                                | High gain by AGC algorithm    |     | 99      |     |      |
| Absolute uncalibrated accuracy <sup>(1)</sup>                                                  |                               |     | $\pm 6$ |     | dB   |
| Step size (LSB value)                                                                          |                               |     | 1       |     | dB   |
| <b>All Other Rates/Formats</b>                                                                 |                               |     |         |     |      |
| Useful RSSI range <sup>(1)</sup>                                                               | Standard mode                 |     | 64      |     | dB   |
|                                                                                                | High-gain mode                |     | 64      |     |      |
| RSSI offset <sup>(1)</sup>                                                                     | Standard mode                 |     | 98      |     | dBm  |
|                                                                                                | High-gain mode                |     | 107     |     |      |
| Absolute uncalibrated accuracy <sup>(1)</sup>                                                  |                               |     | $\pm 3$ |     | dB   |
| Step size (LSB value)                                                                          |                               |     | 1       |     | dB   |

(1) Assuming CC2541 EM reference design. Other RF designs give an offset from the reported value.

## FREQUENCY SYNTHESIZER CHARACTERISTICS

Measured on Texas Instruments CC2541 EM reference design with  $T_A = 25^\circ\text{C}$ ,  $V_{DD} = 3\text{ V}$  and  $f_c = 2440\text{ MHz}$

| PARAMETER                        | TEST CONDITIONS                           | MIN | TYP  | MAX | UNIT   |
|----------------------------------|-------------------------------------------|-----|------|-----|--------|
| Phase noise, unmodulated carrier | At $\pm 1\text{-MHz}$ offset from carrier |     | -109 |     | dBc/Hz |
|                                  | At $\pm 3\text{-MHz}$ offset from carrier |     | -112 |     |        |
|                                  | At $\pm 5\text{-MHz}$ offset from carrier |     | -119 |     |        |

## ANALOG TEMPERATURE SENSOR

Measured on Texas Instruments CC2541 EM reference design with  $T_A = 25^\circ\text{C}$  and  $V_{DD} = 3\text{ V}$

| PARAMETER                            | TEST CONDITIONS                                                                            | MIN | TYP      | MAX | UNIT                |
|--------------------------------------|--------------------------------------------------------------------------------------------|-----|----------|-----|---------------------|
| Output                               | Measured using integrated ADC, internal band-gap voltage reference, and maximum resolution |     | 1480     |     | 12-bit              |
| Temperature coefficient              |                                                                                            |     | 4.5      |     | / $1^\circ\text{C}$ |
| Voltage coefficient                  |                                                                                            |     | 1        |     | 0.1 V               |
| Initial accuracy without calibration |                                                                                            |     | $\pm 10$ |     | $^\circ\text{C}$    |
| Accuracy using 1-point calibration   |                                                                                            |     | $\pm 5$  |     | $^\circ\text{C}$    |
| Current consumption when enabled     |                                                                                            |     | 0.5      |     | mA                  |

## COMPARATOR CHARACTERISTICS

$T_A = 25^\circ\text{C}$ ,  $V_{DD} = 3\text{ V}$ . All measurement results are obtained using the CC2541 reference designs, post-calibration.

| PARAMETER                   | TEST CONDITIONS | MIN | TYP      | MAX | UNIT                         |
|-----------------------------|-----------------|-----|----------|-----|------------------------------|
| Common-mode maximum voltage |                 |     | $V_{DD}$ |     | V                            |
| Common-mode minimum voltage |                 |     | -0.3     |     |                              |
| Input offset voltage        |                 |     | 1        |     | mV                           |
| Offset vs temperature       |                 |     | 16       |     | $\mu\text{V}/^\circ\text{C}$ |
| Offset vs operating voltage |                 |     | 4        |     | mV/V                         |
| Supply current              |                 |     | 230      |     | nA                           |
| Hysteresis                  |                 |     | 0.15     |     | mV                           |

## ADC CHARACTERISTICS

 $T_A = 25^{\circ}\text{C}$  and  $V_{DD} = 3\text{ V}$ 

| PARAMETER                               |                                | TEST CONDITIONS                                                                    | MIN | TYP   | MAX | UNIT |
|-----------------------------------------|--------------------------------|------------------------------------------------------------------------------------|-----|-------|-----|------|
| Input voltage                           |                                | VDD is voltage on AVDD5 pin                                                        | 0   |       | VDD | V    |
| External reference voltage              |                                | VDD is voltage on AVDD5 pin                                                        | 0   |       | VDD | V    |
| External reference voltage differential |                                | VDD is voltage on AVDD5 pin                                                        | 0   |       | VDD | V    |
| Input resistance, signal                |                                | Simulated using 4-MHz clock speed                                                  |     | 197   |     | kΩ   |
| Full-scale signal <sup>(1)</sup>        |                                | Peak-to-peak, defines 0 dBFS                                                       |     | 2.97  |     | V    |
| ENOB <sup>(1)</sup>                     | Effective number of bits       | Single-ended input, 7-bit setting                                                  |     | 5.7   |     | bits |
|                                         |                                | Single-ended input, 9-bit setting                                                  |     | 7.5   |     |      |
|                                         |                                | Single-ended input, 10-bit setting                                                 |     | 9.3   |     |      |
|                                         |                                | Single-ended input, 12-bit setting                                                 |     | 10.3  |     |      |
|                                         |                                | Differential input, 7-bit setting                                                  |     | 6.5   |     |      |
|                                         |                                | Differential input, 9-bit setting                                                  |     | 8.3   |     |      |
|                                         |                                | Differential input, 10-bit setting                                                 |     | 10    |     |      |
|                                         |                                | Differential input, 12-bit setting                                                 |     | 11.5  |     |      |
|                                         |                                | 10-bit setting, clocked by RCOSC                                                   |     | 9.7   |     |      |
|                                         |                                | 12-bit setting, clocked by RCOSC                                                   |     | 10.9  |     |      |
| Useful power bandwidth                  |                                | 7-bit setting, both single and differential                                        |     | 0–20  |     | kHz  |
| THD                                     | Total harmonic distortion      | Single ended input, 12-bit setting, –6 dBFS <sup>(1)</sup>                         |     | –75.2 |     | dB   |
|                                         |                                | Differential input, 12-bit setting, –6 dBFS <sup>(1)</sup>                         |     | –86.6 |     |      |
|                                         | Signal to nonharmonic ratio    | Single-ended input, 12-bit setting <sup>(1)</sup>                                  |     | 70.2  |     | dB   |
|                                         |                                | Differential input, 12-bit setting <sup>(1)</sup>                                  |     | 79.3  |     |      |
|                                         |                                | Single-ended input, 12-bit setting, –6 dBFS <sup>(1)</sup>                         |     | 78.8  |     |      |
|                                         |                                | Differential input, 12-bit setting, –6 dBFS <sup>(1)</sup>                         |     | 88.9  |     |      |
| CMRR                                    | Common-mode rejection ratio    | Differential input, 12-bit setting, 1-kHz sine (0 dBFS), limited by ADC resolution |     | >84   |     | dB   |
| Crosstalk                               |                                | Single ended input, 12-bit setting, 1-kHz sine (0 dBFS), limited by ADC resolution |     | >84   |     | dB   |
| Offset                                  |                                | Midscale                                                                           |     | –3    |     | mV   |
| Gain error                              |                                |                                                                                    |     | 0.68% |     |      |
| DNL                                     | Differential nonlinearity      | 12-bit setting, mean <sup>(1)</sup>                                                |     | 0.05  |     | LSB  |
|                                         |                                | 12-bit setting, maximum <sup>(1)</sup>                                             |     | 0.9   |     |      |
| INL                                     | Integral nonlinearity          | 12-bit setting, mean <sup>(1)</sup>                                                |     | 4.6   |     | LSB  |
|                                         |                                | 12-bit setting, maximum <sup>(1)</sup>                                             |     | 13.3  |     |      |
|                                         |                                | 12-bit setting, mean, clocked by RCOSC                                             |     | 10    |     |      |
|                                         |                                | 12-bit setting, max, clocked by RCOSC                                              |     | 29    |     |      |
| SINAD<br>(–THD+N)                       | Signal-to-noise-and-distortion | Single ended input, 7-bit setting <sup>(1)</sup>                                   |     | 35.4  |     | dB   |
|                                         |                                | Single ended input, 9-bit setting <sup>(1)</sup>                                   |     | 46.8  |     |      |
|                                         |                                | Single ended input, 10-bit setting <sup>(1)</sup>                                  |     | 57.5  |     |      |
|                                         |                                | Single ended input, 12-bit setting <sup>(1)</sup>                                  |     | 66.6  |     |      |
|                                         |                                | Differential input, 7-bit setting <sup>(1)</sup>                                   |     | 40.7  |     |      |
|                                         |                                | Differential input, 9-bit setting <sup>(1)</sup>                                   |     | 51.6  |     |      |
|                                         |                                | Differential input, 10-bit setting <sup>(1)</sup>                                  |     | 61.8  |     |      |
|                                         | Conversion time                | 7-bit setting                                                                      |     | 20    |     | μs   |
|                                         |                                | 9-bit setting                                                                      |     | 36    |     |      |
|                                         |                                | 10-bit setting                                                                     |     | 68    |     |      |
|                                         |                                | 12-bit setting                                                                     |     | 132   |     |      |

(1) Measured with 300-Hz sine-wave input and VDD as reference.

## ADC CHARACTERISTICS (continued)

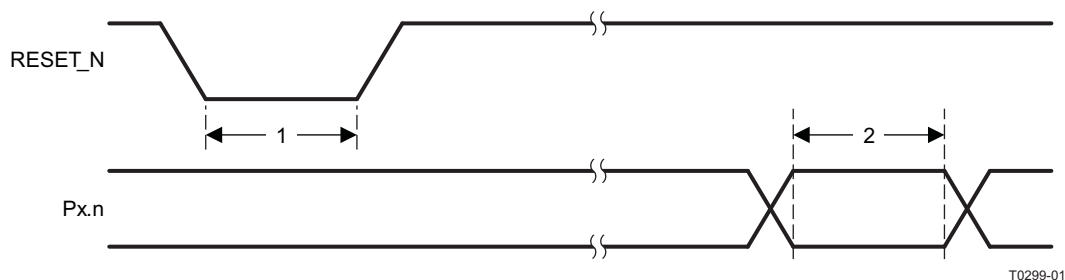
$T_A = 25^\circ\text{C}$  and  $V_{DD} = 3\text{ V}$

| PARAMETER                                  | TEST CONDITIONS | MIN | TYP  | MAX | UNIT                   |
|--------------------------------------------|-----------------|-----|------|-----|------------------------|
| Power consumption                          |                 |     | 1.2  |     | mA                     |
| Internal reference VDD coefficient         |                 |     | 4    |     | mV/V                   |
| Internal reference temperature coefficient |                 |     | 0.4  |     | mV/ $10^\circ\text{C}$ |
| Internal reference voltage                 |                 |     | 1.24 |     | V                      |

## CONTROL INPUT AC CHARACTERISTICS

$T_A = -40^\circ\text{C}$  to  $85^\circ\text{C}$ ,  $V_{DD} = 2\text{ V}$  to  $3.6\text{ V}$

| PARAMETER                                                                      | TEST CONDITIONS                                                                                                                                                                                                                    | MIN | TYP | MAX | UNIT          |
|--------------------------------------------------------------------------------|------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|-----|-----|-----|---------------|
| System clock, $f_{\text{SYSCLK}}$<br>$t_{\text{SYSCLK}} = 1/f_{\text{SYSCLK}}$ | The undivided system clock is 32 MHz when crystal oscillator is used. The undivided system clock is 16 MHz when calibrated 16-MHz RC oscillator is used.                                                                           | 16  |     | 32  | MHz           |
| RESET_N low duration                                                           | See item 1, <a href="#">Figure 2</a> . This is the shortest pulse that is recognized as a complete reset pin request. Note that shorter pulses may be recognized but do not lead to complete reset of all modules within the chip. | 1   |     |     | $\mu\text{s}$ |
| Interrupt pulse duration                                                       | See item 2, <a href="#">Figure 2</a> . This is the shortest pulse that is recognized as an interrupt request.                                                                                                                      | 20  |     |     | ns            |

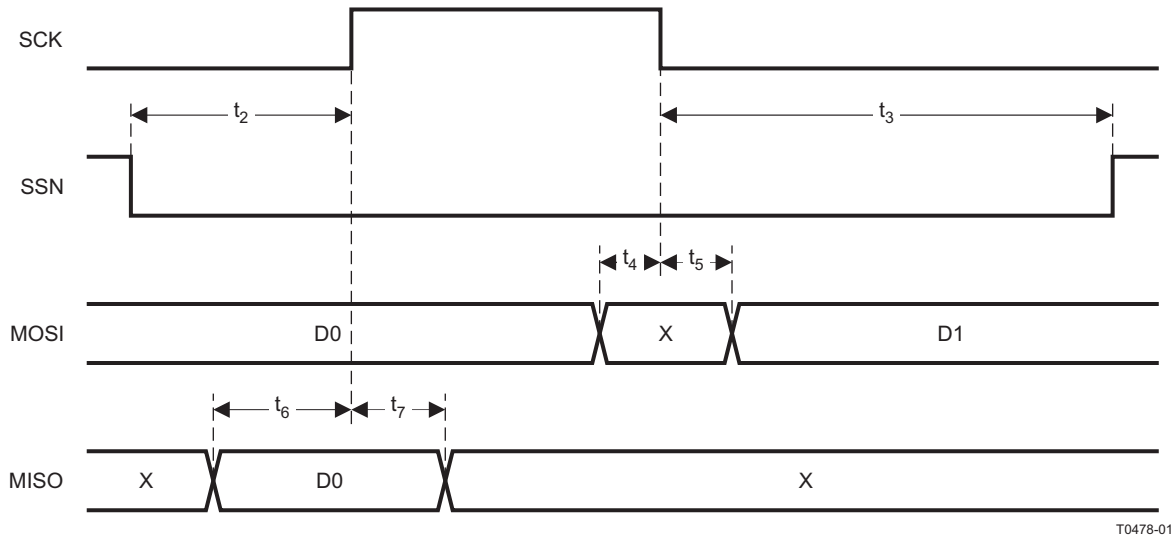


**Figure 2. Control Input AC Characteristics**

## SPI AC CHARACTERISTICS

 $T_A = -40^{\circ}\text{C to } 85^{\circ}\text{C}$ ,  $V_{DD} = 2\text{ V to } 3.6\text{ V}$ 

| PARAMETER           |                 | TEST CONDITIONS      | MIN | TYP | MAX | UNIT |
|---------------------|-----------------|----------------------|-----|-----|-----|------|
| $t_1$               | SCK period      | Master, RX and TX    | 250 |     |     | ns   |
|                     |                 | Slave, RX and TX     | 250 |     |     |      |
|                     | SCK duty cycle  | Master               |     | 50% |     |      |
| $t_2$               | SSN low to SCK  | Master               | 63  |     |     | ns   |
|                     |                 | Slave                | 63  |     |     |      |
| $t_3$               | SCK to SSN high | Master               | 63  |     |     | ns   |
|                     |                 | Slave                | 63  |     |     |      |
| $t_4$               | MOSI early out  | Master, load = 10 pF |     |     | 7   | ns   |
| $t_5$               | MOSI late out   | Master, load = 10 pF |     |     | 10  | ns   |
| $t_6$               | MISO setup      | Master               | 90  |     |     | ns   |
| $t_7$               | MISO hold       | Master               | 10  |     |     | ns   |
|                     | SCK duty cycle  | Slave                |     | 50% |     | ns   |
| $t_{10}$            | MOSI setup      | Slave                | 35  |     |     | ns   |
| $t_{11}$            | MOSI hold       | Slave                | 10  |     |     | ns   |
| $t_9$               | MISO late out   | Slave, load = 10 pF  |     |     | 95  | ns   |
| Operating frequency |                 | Master, TX only      |     |     | 8   | MHz  |
|                     |                 | Master, RX and TX    |     |     | 4   |      |
|                     |                 | Slave, RX only       |     |     | 8   |      |
|                     |                 | Slave, RX and TX     |     |     | 4   |      |



**Figure 3. SPI Master AC Characteristics**

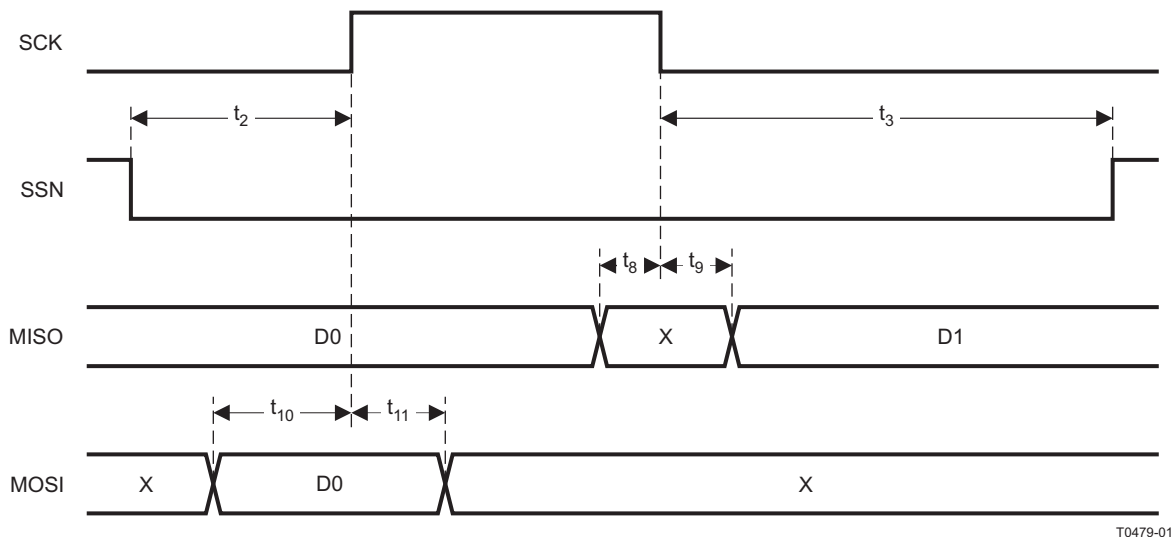


Figure 4. SPI Slave AC Characteristics

## DEBUG INTERFACE AC CHARACTERISTICS

$T_A = -40^{\circ}\text{C}$  to  $85^{\circ}\text{C}$ ,  $V_{DD} = 2\text{ V}$  to  $3.6\text{ V}$

| PARAMETER                                                                 | TEST CONDITIONS | MIN | TYP | MAX | UNIT |
|---------------------------------------------------------------------------|-----------------|-----|-----|-----|------|
| $f_{\text{clk\_dbg}}$ Debug clock frequency (see Figure 5)                |                 |     |     | 12  | MHz  |
| $t_1$ Allowed high pulse on clock (see Figure 5)                          |                 | 35  |     |     | ns   |
| $t_2$ Allowed low pulse on clock (see Figure 5)                           |                 | 35  |     |     | ns   |
| $t_3$ EXT_RESET_N low to first falling edge on debug clock (see Figure 7) |                 | 167 |     |     | ns   |
| $t_4$ Falling edge on clock to EXT_RESET_N high (see Figure 7)            |                 | 83  |     |     | ns   |
| $t_5$ EXT_RESET_N high to first debug command (see Figure 7)              |                 | 83  |     |     | ns   |
| $t_6$ Debug data setup (see Figure 6)                                     |                 | 2   |     |     | ns   |
| $t_7$ Debug data hold (see Figure 6)                                      |                 | 4   |     |     | ns   |
| $t_8$ Clock-to-data delay (see Figure 6)                                  | Load = 10 pF    |     |     | 30  | ns   |

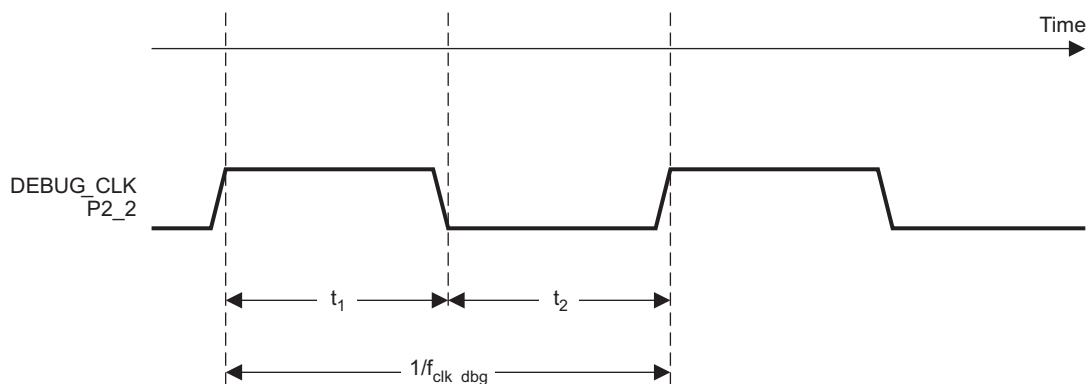
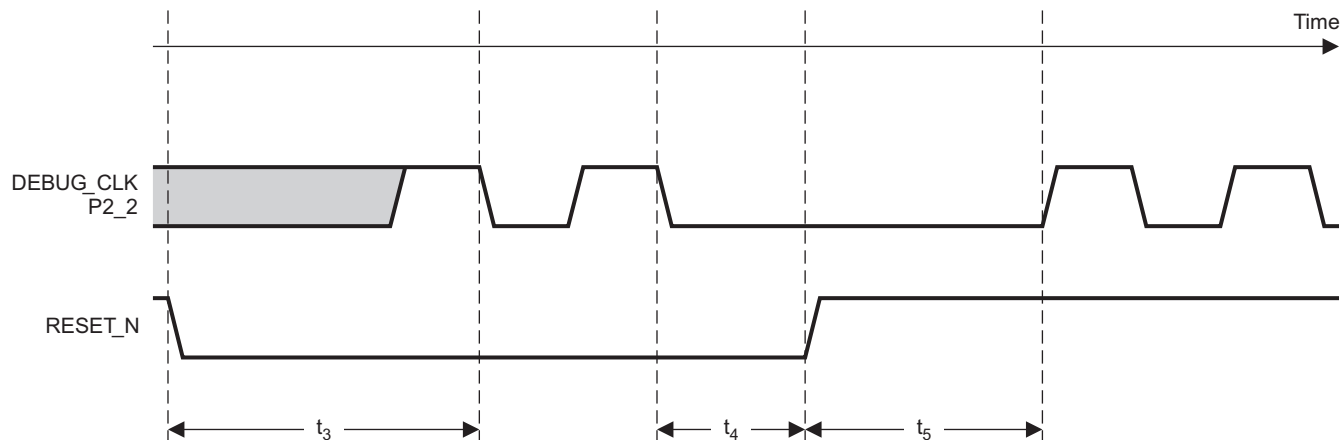


Figure 5. Debug Clock – Basic Timing



T0437-01

Figure 6. Debug Enable Timing

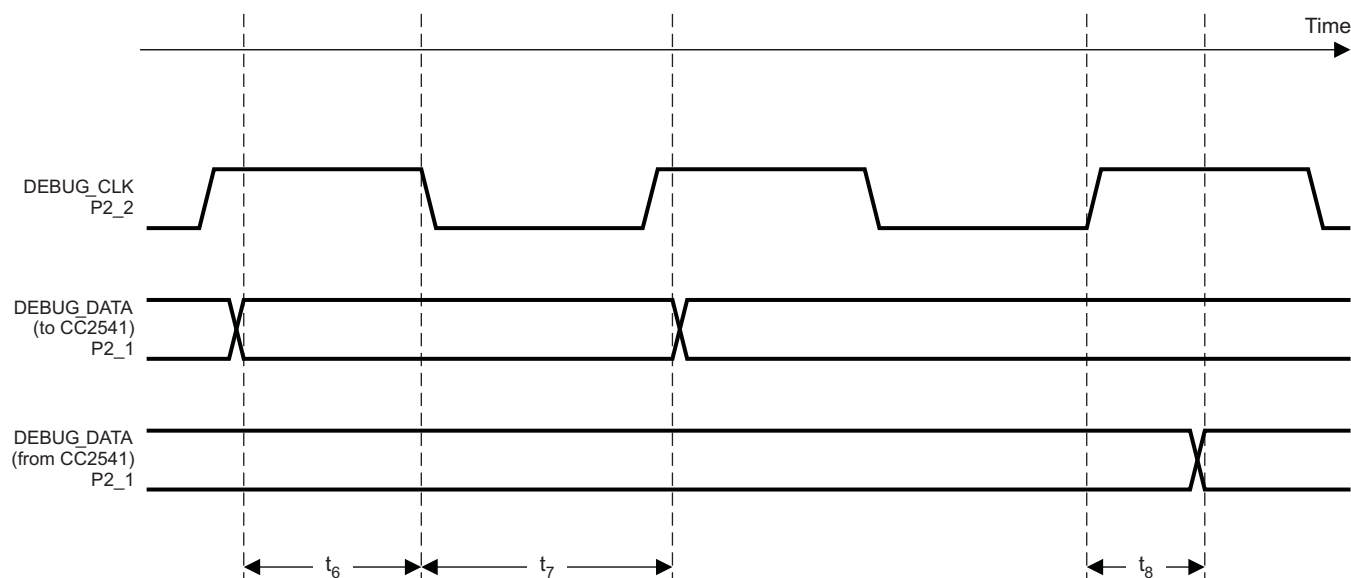


Figure 7. Data Setup and Hold Timing

## TIMER INPUTS AC CHARACTERISTICS

$T_A = -40^{\circ}\text{C}$  to  $85^{\circ}\text{C}$ ,  $V_{DD} = 2\text{ V}$  to  $3.6\text{ V}$

| PARAMETER                    | TEST CONDITIONS                                                                                                                                         | MIN | TYP | MAX | UNIT                |
|------------------------------|---------------------------------------------------------------------------------------------------------------------------------------------------------|-----|-----|-----|---------------------|
| Input capture pulse duration | Synchronizers determine the shortest input pulse that can be recognized. The synchronizers operate at the current system clock rate (16 MHz or 32 MHz). | 1.5 |     |     | $t_{\text{SYSCLK}}$ |

## DC CHARACTERISTICS

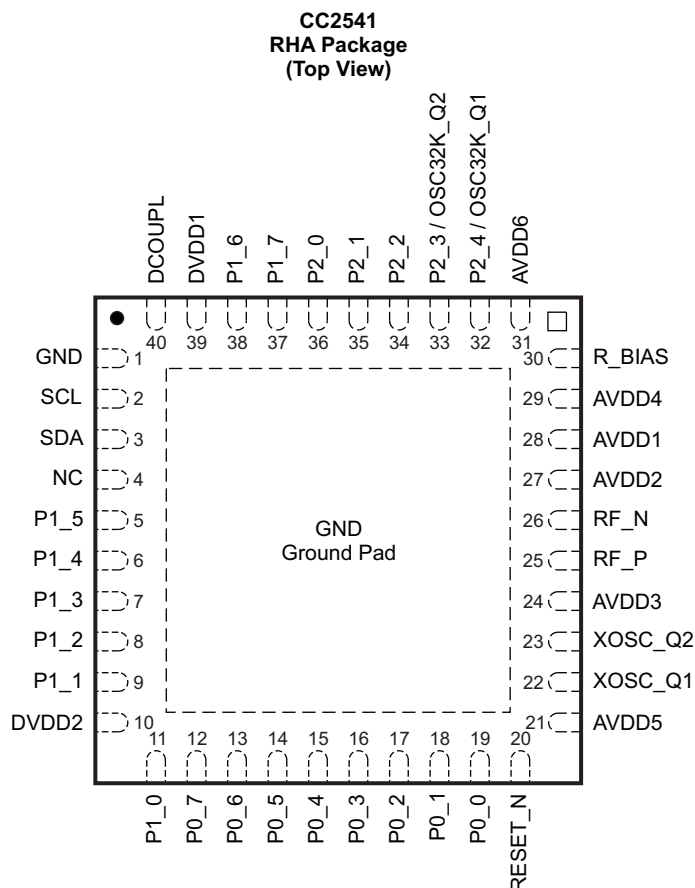
 $T_A = 25^\circ\text{C}$ ,  $V_{DD} = 3\text{ V}$ 

| PARAMETER                             | TEST CONDITIONS   | MIN | TYP | MAX | UNIT       |
|---------------------------------------|-------------------|-----|-----|-----|------------|
| Logic-0 input voltage                 |                   |     |     | 0.5 | V          |
| Logic-1 input voltage                 |                   | 2.4 |     |     | V          |
| Logic-0 input current                 | Input equals 0 V  | -50 |     | 50  | nA         |
| Logic-1 input current                 | Input equals VDD  | -50 |     | 50  | nA         |
| I/O-pin pullup and pulldown resistors |                   |     | 20  |     | k $\Omega$ |
| Logic-0 output voltage, 4- mA pins    | Output load 4 mA  |     |     | 0.5 | V          |
| Logic-1 output voltage, 4-mA pins     | Output load 4 mA  | 2.5 |     |     | V          |
| Logic-0 output voltage, 20- mA pins   | Output load 20 mA |     |     | 0.5 | V          |
| Logic-1 output voltage, 20-mA pins    | Output load 20 mA | 2.5 |     |     | V          |

## DEVICE INFORMATION

### PIN DESCRIPTIONS

The CC2541 pinout is shown in [Figure 8](#) and a short description of the pins follows.



NOTE: The exposed ground pad must be connected to a solid ground plane, as this is the ground connection for the chip.

**Figure 8. Pinout Top View**

### PIN DESCRIPTIONS

| PIN NAME           | PIN | PIN TYPE                              | DESCRIPTION                                                                                                       |
|--------------------|-----|---------------------------------------|-------------------------------------------------------------------------------------------------------------------|
| AVDD1              | 28  | Power (analog)                        | 2-V–3.6-V analog power-supply connection                                                                          |
| AVDD2              | 27  | Power (analog)                        | 2-V–3.6-V analog power-supply connection                                                                          |
| AVDD3              | 24  | Power (analog)                        | 2-V–3.6-V analog power-supply connection                                                                          |
| AVDD4              | 29  | Power (analog)                        | 2-V–3.6-V analog power-supply connection                                                                          |
| AVDD5              | 21  | Power (analog)                        | 2-V–3.6-V analog power-supply connection                                                                          |
| AVDD6              | 31  | Power (analog)                        | 2-V–3.6-V analog power-supply connection                                                                          |
| DCOUP_L            | 40  | Power (digital)                       | 1.8-V digital power-supply decoupling. Do not use for supplying external circuits.                                |
| DVDD1              | 39  | Power (digital)                       | 2-V–3.6-V digital power-supply connection                                                                         |
| DVDD2              | 10  | Power (digital)                       | 2-V–3.6-V digital power-supply connection                                                                         |
| GND                | 1   | Ground pin                            | Connect to GND                                                                                                    |
| GND                | —   | Ground                                | The ground pad must be connected to a solid ground plane.                                                         |
| NC                 | 4   | Unused pins                           | Not connected                                                                                                     |
| P0_0               | 19  | Digital I/O                           | Port 0.0                                                                                                          |
| P0_1               | 18  | Digital I/O                           | Port 0.1                                                                                                          |
| P0_2               | 17  | Digital I/O                           | Port 0.2                                                                                                          |
| P0_3               | 16  | Digital I/O                           | Port 0.3                                                                                                          |
| P0_4               | 15  | Digital I/O                           | Port 0.4                                                                                                          |
| P0_5               | 14  | Digital I/O                           | Port 0.5                                                                                                          |
| P0_6               | 13  | Digital I/O                           | Port 0.6                                                                                                          |
| P0_7               | 12  | Digital I/O                           | Port 0.7                                                                                                          |
| P1_0               | 11  | Digital I/O                           | Port 1.0 – 20-mA drive capability                                                                                 |
| P1_1               | 9   | Digital I/O                           | Port 1.1 – 20-mA drive capability                                                                                 |
| P1_2               | 8   | Digital I/O                           | Port 1.2                                                                                                          |
| P1_3               | 7   | Digital I/O                           | Port 1.3                                                                                                          |
| P1_4               | 6   | Digital I/O                           | Port 1.4                                                                                                          |
| P1_5               | 5   | Digital I/O                           | Port 1.5                                                                                                          |
| P1_6               | 38  | Digital I/O                           | Port 1.6                                                                                                          |
| P1_7               | 37  | Digital I/O                           | Port 1.7                                                                                                          |
| P2_0               | 36  | Digital I/O                           | Port 2.0                                                                                                          |
| P2_1/DD            | 35  | Digital I/O                           | Port 2.1 / debug data                                                                                             |
| P2_2/DC            | 34  | Digital I/O                           | Port 2.2 / debug clock                                                                                            |
| P2_3/<br>OSC32K_Q2 | 33  | Digital I/O, Analog I/O               | Port 2.3/32.768 kHz XOSC                                                                                          |
| P2_4/<br>OSC32K_Q1 | 32  | Digital I/O, Analog I/O               | Port 2.4/32.768 kHz XOSC                                                                                          |
| RBIAS              | 30  | Analog I/O                            | External precision bias resistor for reference current                                                            |
| RESET_N            | 20  | Digital input                         | Reset, active-low                                                                                                 |
| RF_N               | 26  | RF I/O                                | Negative RF input signal to LNA during RX<br>Negative RF output signal from PA during TX                          |
| RF_P               | 25  | RF I/O                                | Positive RF input signal to LNA during RX<br>Positive RF output signal from PA during TX                          |
| SCL                | 2   | I <sup>2</sup> C clock or digital I/O | Can be used as I <sup>2</sup> C clock pin or digital I/O. Leave floating if not used. If grounded disable pull up |
| SDA                | 3   | I <sup>2</sup> C clock or digital I/O | Can be used as I <sup>2</sup> C data pin or digital I/O. Leave floating if not used. If grounded disable pull up  |
| XOSC_Q1            | 22  | Analog I/O                            | 32-MHz crystal oscillator pin 1 or external clock input                                                           |
| XOSC_Q2            | 23  | Analog I/O                            | 32-MHz crystal oscillator pin 2                                                                                   |

## BLOCK DIAGRAM

A block diagram of the CC2541 is shown in Figure 9. The modules can be roughly divided into one of three categories: CPU-related modules; modules related to power, test, and clock distribution; and radio-related modules. In the following subsections, a short description of each module is given.

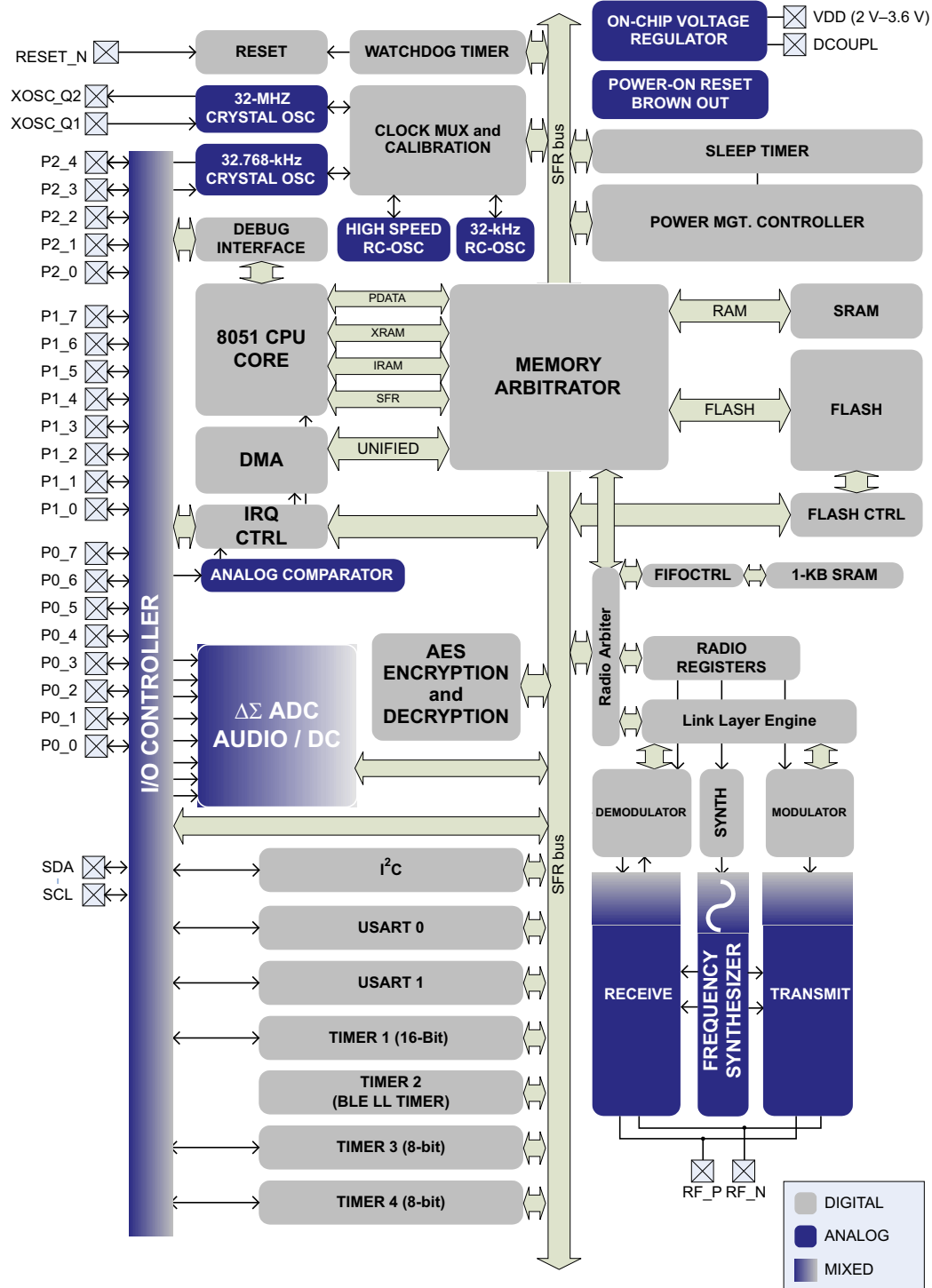


Figure 9. CC2541 Block Diagram

## BLOCK DESCRIPTIONS

A block diagram of the CC2541 is shown in [Figure 9](#). The modules can be roughly divided into one of three categories: CPU-related modules; modules related to power, test, and clock distribution; and radio-related modules. In the following subsections, a short description of each module is given.

### CPU and Memory

The **8051 CPU core** is a single-cycle 8051-compatible core. It has three different memory access busses (SFR, DATA, and CODE/XDATA), a debug interface, and an 18-input extended interrupt unit.

The **memory arbiter** is at the heart of the system, as it connects the CPU and DMA controller with the physical memories and all peripherals through the SFR bus. The memory arbiter has four memory-access points, access of which can map to one of three physical memories: an SRAM, flash memory, and XREG/SFR registers. It is responsible for performing arbitration and sequencing between simultaneous memory accesses to the same physical memory.

The **SFR bus** is drawn conceptually in [Figure 9](#) as a common bus that connects all hardware peripherals to the memory arbiter. The SFR bus in the block diagram also provides access to the radio registers in the radio register bank, even though these are indeed mapped into XDATA memory space.

The **8-KB SRAM** maps to the DATA memory space and to parts of the XDATA memory spaces. The SRAM is an ultralow-power SRAM that retains its contents even when the digital part is powered off (power mode 2 and mode 3).

The **128/256 KB flash block** provides in-circuit programmable non-volatile program memory for the device, and maps into the CODE and XDATA memory spaces.

### Peripherals

Writing to the flash block is performed through a **flash controller** that allows page-wise erasure and 4-bytewise programming. See User Guide for details on the flash controller.

A versatile five-channel **DMA controller** is available in the system, accesses memory using the XDATA memory space, and thus has access to all physical memories. Each channel (trigger, priority, transfer mode, addressing mode, source and destination pointers, and transfer count) is configured with DMA descriptors that can be located anywhere in memory. Many of the hardware peripherals (AES core, flash controller, USARTs, timers, ADC interface, etc.) can be used with the DMA controller for efficient operation by performing data transfers between a single SFR or XREG address and flash/SRAM.

Each CC2541 contains a unique 48-bit IEEE address that can be used as the public device address for a *Bluetooth* device. Designers are free to use this address, or provide their own, as described in the *Bluetooth* specification.

The **interrupt controller** services a total of 18 interrupt sources, divided into six interrupt groups, each of which is associated with one of four interrupt priorities. I/O and sleep timer interrupt requests are serviced even if the device is in a sleep mode (power modes 1 and 2) by bringing the CC2541 back to the active mode.

The **debug interface** implements a proprietary two-wire serial interface that is used for in-circuit debugging. Through this debug interface, it is possible to erase or program the entire flash memory, control which oscillators are enabled, stop and start execution of the user program, execute instructions on the 8051 core, set code breakpoints, and single-step through instructions in the code. Using these techniques, it is possible to perform in-circuit debugging and external flash programming elegantly.

The **I/O controller** is responsible for all general-purpose I/O pins. The CPU can configure whether peripheral modules control certain pins or whether they are under software control, and if so, whether each pin is configured as an input or output and if a pullup or pulldown resistor in the pad is connected. Each peripheral that connects to the I/O pins can choose between two different I/O pin locations to ensure flexibility in various applications.

The **sleep timer** is an ultralow-power timer that can either use an external 32.768-kHz crystal oscillator or an internal 32.753-kHz RC oscillator. The sleep timer runs continuously in all operating modes except power mode 3. Typical applications of this timer are as a real-time counter or as a wake-up timer to get out of power mode 1 or mode 2.

A built-in **watchdog timer** allows the CC2541 to reset itself if the firmware hangs. When enabled by software, the watchdog timer must be cleared periodically; otherwise, it resets the device when it times out.

**Timer 1** is a 16-bit timer with timer/counter/PWM functionality. It has a programmable prescaler, a 16-bit period value, and five individually programmable counter/capture channels, each with a 16-bit compare value. Each of the counter/capture channels can be used as a PWM output or to capture the timing of edges on input signals. It can also be configured in IR generation mode, where it counts timer 3 periods and the output is ANDed with the output of timer 3 to generate modulated consumer IR signals with minimal CPU interaction.

**Timer 2** is a 40-bit timer. It has a 16-bit counter with a configurable timer period and a 24-bit overflow counter that can be used to keep track of the number of periods that have transpired. A 40-bit capture register is also used to record the exact time at which a start-of-frame delimiter is received/transmitted or the exact time at which transmission ends. There are two 16-bit output compare registers and two 24-bit overflow compare registers that can be used to give exact timing for start of RX or TX to the radio or general interrupts.

**Timer 3 and timer 4** are 8-bit timers with timer/counter/PWM functionality. They have a programmable prescaler, an 8-bit period value, and one programmable counter channel with an 8-bit compare value. Each of the counter channels can be used as PWM output.

**USART 0 and USART 1** are each configurable as either an SPI master/slave or a UART. They provide double buffering on both RX and TX and hardware flow control and are thus well suited to high-throughput full-duplex applications. Each USART has its own high-precision baud-rate generator, thus leaving the ordinary timers free for other uses. When configured as SPI slaves, the USARTs sample the input signal using SCK directly instead of using some oversampling scheme, and are thus well-suited for high data rates.

The **AES encryption/decryption core** allows the user to encrypt and decrypt data using the AES algorithm with 128-bit keys. The AES core also supports ECB, CBC, CFB, OFB, CTR, and CBC-MAC, as well as hardware support for CCM.

The **ADC** supports 7 to 12 bits of resolution with a corresponding range of bandwidths from 30-kHz to 4-kHz, respectively. DC and audio conversions with up to eight input channels (I/O controller pins) are possible. The inputs can be selected as single-ended or differential. The reference voltage can be internal, AVDD, or a single-ended or differential external signal. The ADC also has a temperature-sensor input channel. The ADC can automate the process of periodic sampling or conversion over a sequence of channels.

The **I<sup>2</sup>C** module provides a digital peripheral connection with two pins and supports both master and slave operation. I<sup>2</sup>C support is compliant with the NXP I<sup>2</sup>C specification version 2.1 and supports standard mode (up to 100 kbps) and fast mode (up to 400 kbps). In addition, 7-bit device addressing modes are supported, as well as master and slave modes.

The ultralow-power **analog comparator** enables applications to wake up from PM2 or PM3 based on an analog signal. Both inputs are brought out to pins; the reference voltage must be provided externally. The comparator output is connected to the I/O controller interrupt detector and can be treated by the MCU as a regular I/O pin interrupt.

## TYPICAL CHARACTERISTICS

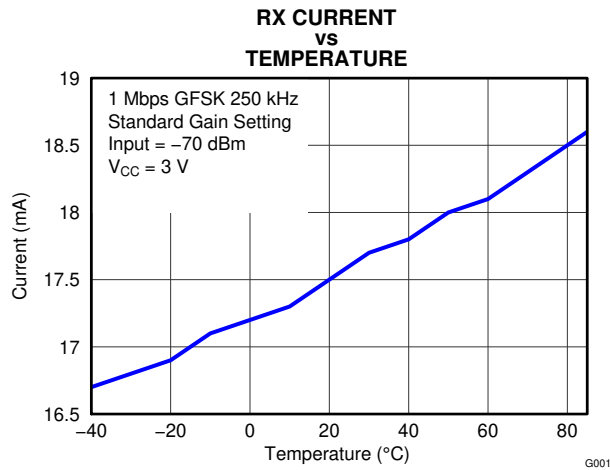


Figure 10.

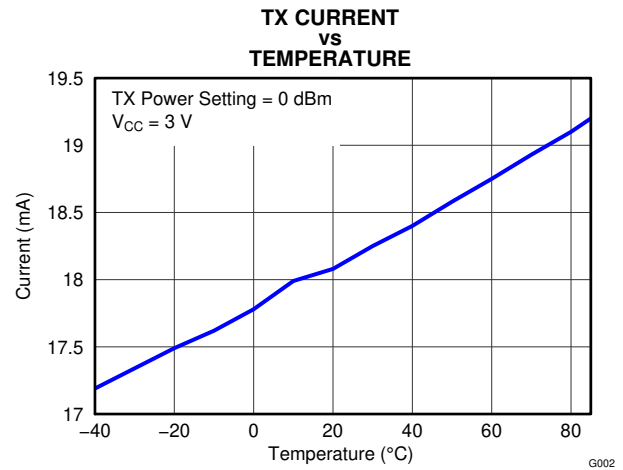


Figure 11.

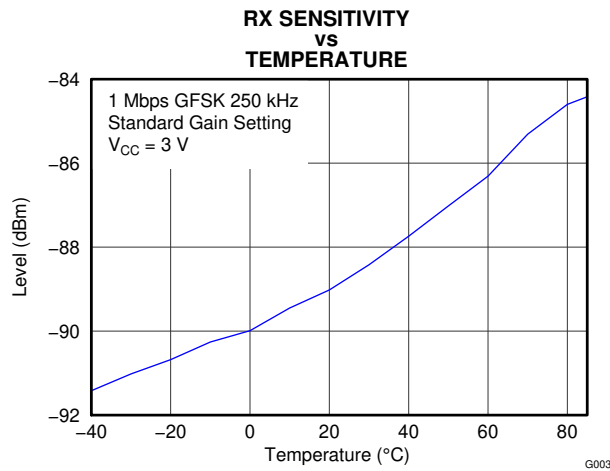


Figure 12.

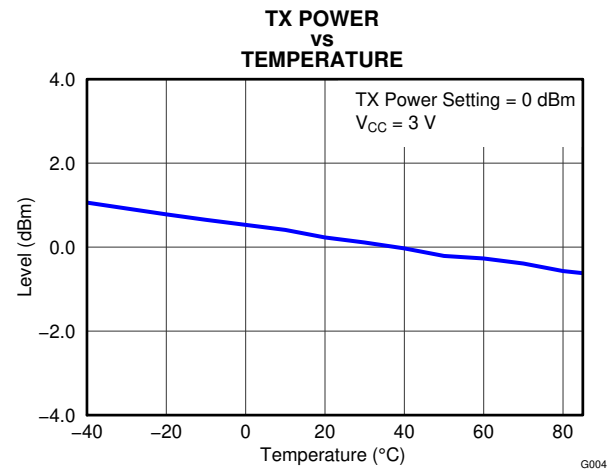


Figure 13.

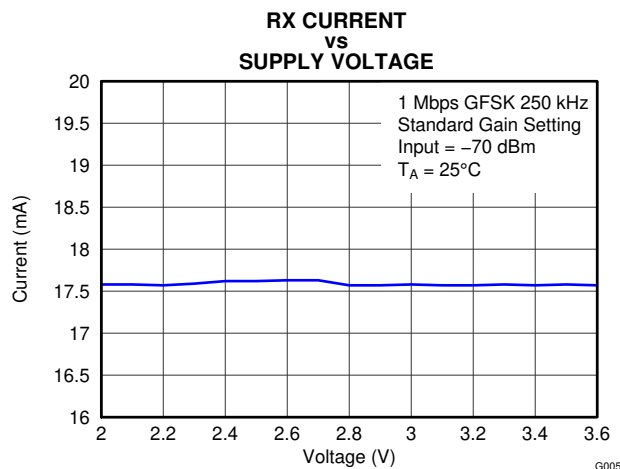


Figure 14.

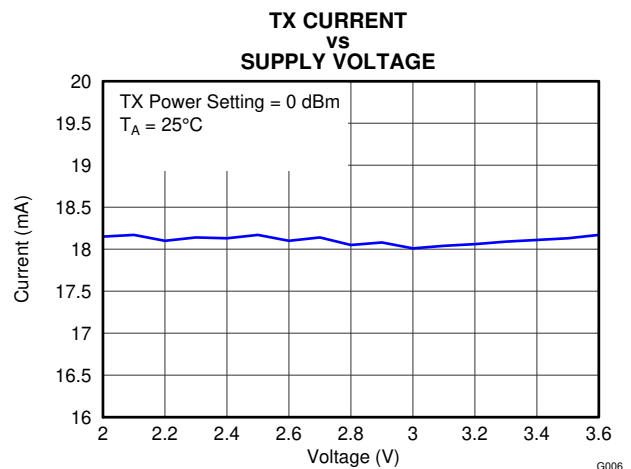
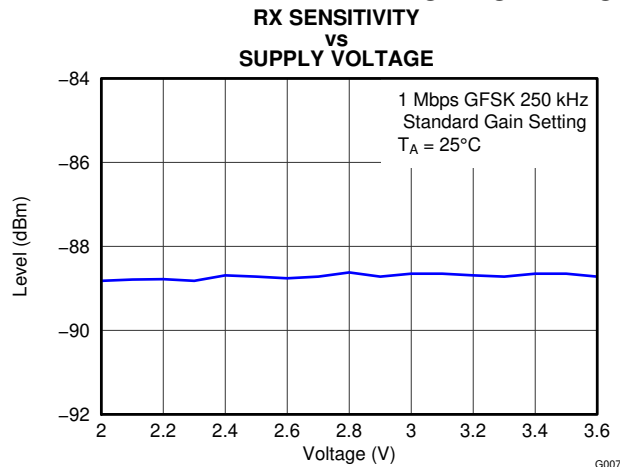
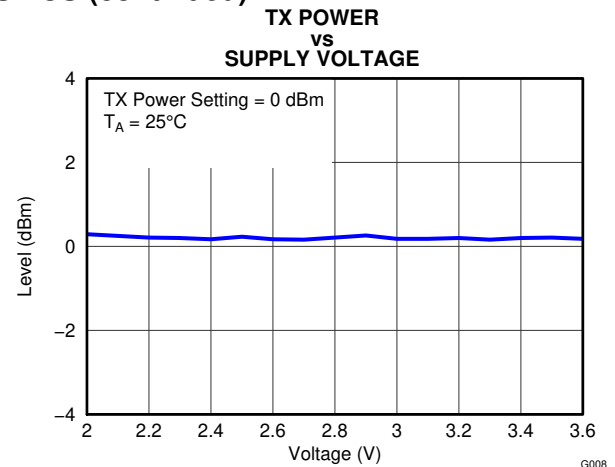
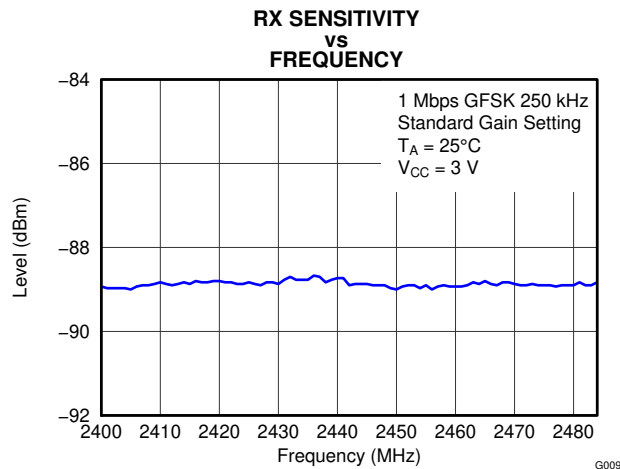
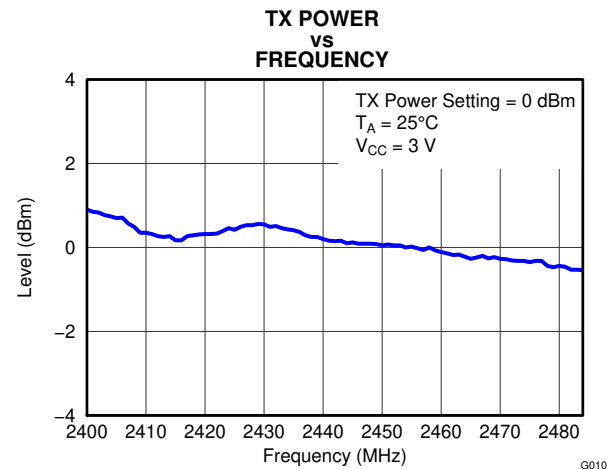


Figure 15.

**TYPICAL CHARACTERISTICS (continued)****Figure 16.****Figure 17.****Figure 18.****Figure 19.****Table 1. Output Power<sup>(1)(2)</sup>**

| TXPOWER Setting | Typical Output Power (dBm) |
|-----------------|----------------------------|
| 0xE1            | 0                          |
| 0xD1            | -2                         |
| 0xC1            | -4                         |
| 0xB1            | -6                         |
| 0xA1            | -8                         |
| 0x91            | -10                        |
| 0x81            | -12                        |
| 0x71            | -14                        |
| 0x61            | -16                        |
| 0x51            | -18                        |
| 0x41            | -20                        |
| 0x31            | -23                        |

(1) Measured on Texas Instruments CC2541 EM reference design with  $T_A = 25^\circ\text{C}$ ,  $V_{DD} = 3\text{ V}$  and  $f_c = 2440\text{ MHz}$ . See [SWRU191](#) for recommended register settings.

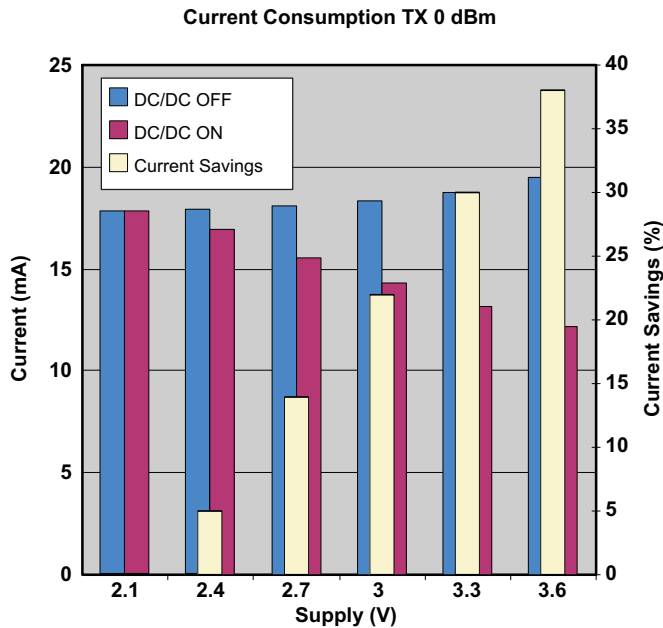
(2) 1 Mbps, GFSK, 250-kHz deviation, Bluetooth™ low energy mode, 1% BER

**Table 2. Output Power and Current Consumption**

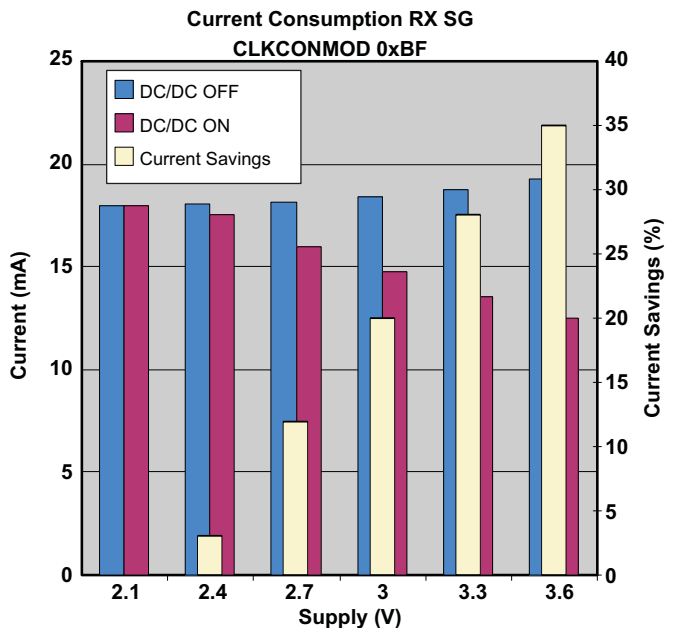
| Typical Output Power (dBm) | Typical Current Consumption (mA) <sup>(1)</sup> | Typical Current Consumption With TPS62730 (mA) <sup>(2)</sup> |
|----------------------------|-------------------------------------------------|---------------------------------------------------------------|
| 0                          | 18.2                                            | 14.3                                                          |
| -20                        | 16.8                                            | 13.1                                                          |

- (1) Measured on Texas Instruments CC2541 EM reference design with  $T_A = 25^\circ\text{C}$ ,  $V_{DD} = 3\text{ V}$  and  $f_c = 2440\text{ MHz}$ . See [SWRU191](#) for recommended register settings.
- (2) Measured on Texas Instruments CC2541 TPS62730 EM reference design with  $T_A = 25^\circ\text{C}$ ,  $V_{DD} = 3\text{ V}$  and  $f_c = 2440\text{ MHz}$ . See [SWRU191](#) for recommended register settings.

## TYPICAL CURRENT SAVINGS WHEN USING TPS62730



**Figure 20. Current Savings in TX at Room Temperature**

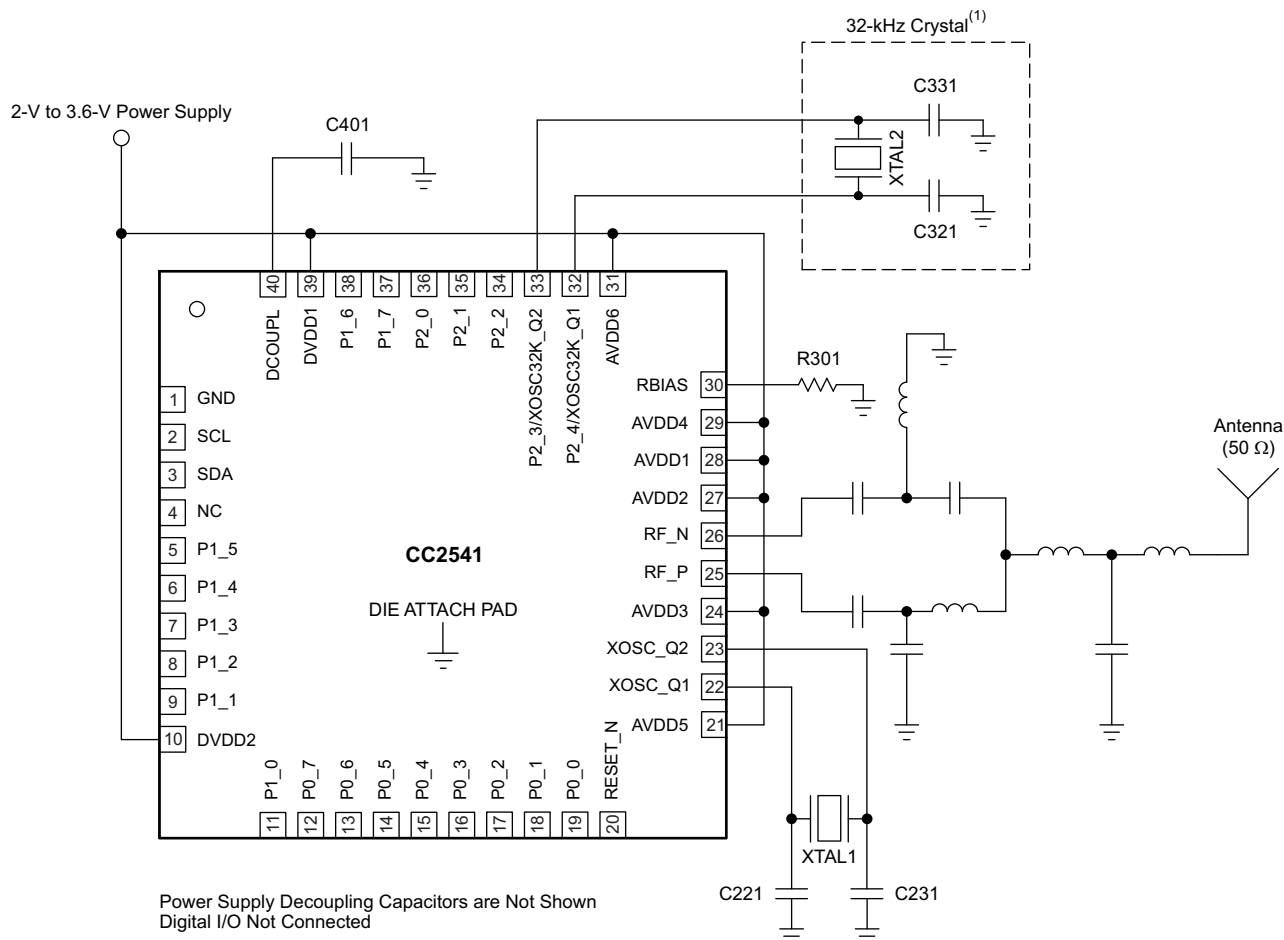


**Figure 21. Current Savings in RX at Room Temperature**

The application note ([SWRA365](#)) has information regarding the CC2541 and TPS62730 combo board and the current savings that can be achieved using the combo board.

## APPLICATION INFORMATION

Few external components are required for the operation of the CC2541. A typical application circuit is shown in Figure 22.



(1) 32-kHz crystal is mandatory when running the BLE protocol stack in low-power modes, except if the link layer is in the standby state (Vol. 6 Part B Section 1.1 in [1]).

NOTE: Different antenna alternatives will be provided as reference designs.

**Figure 22. CC2541 Application Circuit**

**Table 3. Overview of External Components (Excluding Supply Decoupling Capacitors)**

| Component | Description                                                           | Value         |
|-----------|-----------------------------------------------------------------------|---------------|
| C401      | Decoupling capacitor for the internal 1.8-V digital voltage regulator | 1 $\mu$ F     |
| R301      | Precision resistor $\pm 1\%$ , used for internal biasing              | 56 k $\Omega$ |

### Input/Output Matching

When using an unbalanced antenna such as a monopole, a balun should be used to optimize performance. The balun can be implemented using low-cost discrete inductors and capacitors. See reference design, CC2541EM, for recommended balun.

## Crystal

An external 32-MHz crystal, XTAL1, with two loading capacitors (C221 and C231) is used for the 32-MHz crystal oscillator. See [32-MHz CRYSTAL OSCILLATOR](#) for details. The load capacitance seen by the 32-MHz crystal is given by:

$$C_L = \frac{1}{\frac{1}{C_{221}} + \frac{1}{C_{231}}} + C_{\text{parasitic}} \quad (1)$$

XTAL2 is an optional 32.768-kHz crystal, with two loading capacitors (C321 and C331) used for the 32.768-kHz crystal oscillator. The 32.768-kHz crystal oscillator is used in applications where both very low sleep-current consumption and accurate wake-up times are needed. The load capacitance seen by the 32.768-kHz crystal is given by:

$$C_L = \frac{1}{\frac{1}{C_{321}} + \frac{1}{C_{331}}} + C_{\text{parasitic}} \quad (2)$$

A series resistor may be used to comply with the ESR requirement.

## On-Chip 1.8-V Voltage Regulator Decoupling

The 1.8-V on-chip voltage regulator supplies the 1.8-V digital logic. This regulator requires a decoupling capacitor (C401) for stable operation.

## Power-Supply Decoupling and Filtering

Proper power-supply decoupling must be used for optimum performance. The placement and size of the decoupling capacitors and the power supply filtering are very important to achieve the best performance in an application. TI provides a compact reference design that should be followed very closely.

## References

1. *Bluetooth®* Core Technical Specification document, version 4.0  
[http://www.bluetooth.com/SiteCollectionDocuments/Core\\_V40.zip](http://www.bluetooth.com/SiteCollectionDocuments/Core_V40.zip)
2. CC253x System-on-Chip Solution for 2.4-GHz IEEE 802.15.4 and ZigBee® Applications/CC2541 System-on-Chip Solution for 2.4-GHz *Bluetooth* low energy Applications ([SWRU191](#))
3. Current Savings in CC254x Using the TPS62730 ([SWRA365](#)).

## Additional Information

Texas Instruments offers a wide selection of cost-effective, low-power RF solutions for proprietary and standard-based wireless applications for use in industrial and consumer applications. Our selection includes RF transceivers, RF transmitters, RF front ends, and System-on-Chips as well as various software solutions for the sub-1- and 2.4-GHz frequency bands.

In addition, Texas Instruments provides a large selection of support collateral such as development tools, technical documentation, reference designs, application expertise, customer support, third-party and university programs.

The Low-Power RF E2E Online Community provides technical support forums, videos and blogs, and the chance to interact with fellow engineers from all over the world.

With a broad selection of product solutions, end application possibilities, and a range of technical support, Texas Instruments offers the broadest low-power RF portfolio. We make RF easy!

The following subsections point to where to find more information.

## Texas Instruments Low-Power RF Web Site

- Forums, videos, and blogs
- RF design help
- E2E interaction

Join us today at [www.ti.com/lprf-forum](http://www.ti.com/lprf-forum).

## Texas Instruments Low-Power RF Developer Network

Texas Instruments has launched an extensive network of low-power RF development partners to help customers speed up their application development. The network consists of recommended companies, RF consultants, and independent design houses that provide a series of hardware module products and design services, including:

- RF circuit, low-power RF, and ZigBee® design services
- Low-power RF and ZigBee module solutions and development tools
- RF certification services and RF circuit manufacturing

Need help with modules, engineering services or development tools?

Search the Low-Power RF Developer Network tool to find a suitable partner.

[www.ti.com/lprfnetwork](http://www.ti.com/lprfnetwork)

## Low-Power RF eNewsletter

The Low-Power RF eNewsletter keeps you up-to-date on new products, news releases, developers' news, and other news and events associated with low-power RF products from TI. The Low-Power RF eNewsletter articles include links to get more online information.

Sign up today on

[www.ti.com/lprfnewsletter](http://www.ti.com/lprfnewsletter)

## REVISION HISTORY

| Changes from Original (January 2012) to Revision A                                                 | Page |
|----------------------------------------------------------------------------------------------------|------|
| • Changed data sheet status from Product Preview to Production Data .....                          | 1    |
| Changes from Revision A (February 2012) to Revision B                                              | Page |
| • Changed the Temperature coefficient Unit value From: mV/°C To: / 0.1°C .....                     | 10   |
| • Changed <a href="#">Figure 22</a> text From: Optional 32-kHz Crystal To: 32-kHz Crystal .....    | 24   |
| Changes from Revision B (August 2012) to Revision C                                                | Page |
| • Changed the "Internal reference voltage" TYP value From 1.15 V To: 1.24 V .....                  | 12   |
| • Changed pin XOSC_Q1 Pin Type From Analog O To: Analog I/O, and changed the Pin Description ..... | 17   |
| • Changed pin XOSC_Q2 Pin Type From Analog O To: Analog I/O .....                                  | 17   |
| Changes from Revision C (November 2012) to Revision D                                              | Page |
| • Changed the RF TRANSMIT SECTION, Output power TYP value From: –20 To: –23 .....                  | 8    |
| • Changed the RF TRANSMIT SECTION, Programmable output power range TYP value From: 20 To: 23 ..... | 8    |
| • Added row 0x31 to <a href="#">Table 1</a> .....                                                  | 22   |

## PACKAGING INFORMATION

| Orderable Device | Status<br>(1) | Package Type | Package<br>Drawing | Pins | Package<br>Qty | Eco Plan<br>(2)            | Lead/Ball Finish<br>(6)        | MSL Peak Temp<br>(3) | Op Temp (°C) | Device Marking<br>(4/5) | Samples                 |
|------------------|---------------|--------------|--------------------|------|----------------|----------------------------|--------------------------------|----------------------|--------------|-------------------------|-------------------------|
| CC2541F128RHAR   | ACTIVE        | VQFN         | RHA                | 40   | 2500           | Green (RoHS<br>& no Sb/Br) | NIPDAU   NIPDAUAG              | Level-3-260C-168 HR  | -40 to 85    | CC2541<br>F128          | <a href="#">Samples</a> |
| CC2541F128RHAT   | ACTIVE        | VQFN         | RHA                | 40   | 250            | Green (RoHS<br>& no Sb/Br) | NIPDAU   NIPDAUAG              | Level-3-260C-168 HR  | -40 to 85    | CC2541<br>F128          | <a href="#">Samples</a> |
| CC2541F256RHAR   | ACTIVE        | VQFN         | RHA                | 40   | 2500           | Green (RoHS<br>& no Sb/Br) | Call TI   NIPDAUAG<br>  NIPDAU | Level-3-260C-168 HR  | -40 to 85    | CC2541<br>F256          | <a href="#">Samples</a> |
| CC2541F256RHAT   | ACTIVE        | VQFN         | RHA                | 40   | 250            | Green (RoHS<br>& no Sb/Br) | Call TI   NIPDAUAG<br>  NIPDAU | Level-3-260C-168 HR  | -40 to 85    | CC2541<br>F256          | <a href="#">Samples</a> |
| HPA01215RHAR     | ACTIVE        | VQFN         | RHA                | 40   | 2500           | Green (RoHS<br>& no Sb/Br) | NIPDAU                         | Level-3-260C-168 HR  | -40 to 85    | CC2541<br>F128          | <a href="#">Samples</a> |
| HPA01216RHAR     | ACTIVE        | VQFN         | RHA                | 40   | 2500           | Green (RoHS<br>& no Sb/Br) | NIPDAU                         | Level-3-260C-168 HR  | -40 to 85    | CC2541<br>F256          | <a href="#">Samples</a> |

(1) The marketing status values are defined as follows:

**ACTIVE:** Product device recommended for new designs.

**LIFEBUY:** TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.

**NRND:** Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.

**PREVIEW:** Device has been announced but is not in production. Samples may or may not be available.

**OBSOLETE:** TI has discontinued the production of the device.

(2) **RoHS:** TI defines "RoHS" to mean semiconductor products that are compliant with the current EU RoHS requirements for all 10 RoHS substances, including the requirement that RoHS substance do not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, "RoHS" products are suitable for use in specified lead-free processes. TI may reference these types of products as "Pb-Free".

**RoHS Exempt:** TI defines "RoHS Exempt" to mean products that contain lead but are compliant with EU RoHS pursuant to a specific EU RoHS exemption.

**Green:** TI defines "Green" to mean the content of Chlorine (Cl) and Bromine (Br) based flame retardants meet JS709B low halogen requirements of <=1000ppm threshold. Antimony trioxide based flame retardants must also meet the <=1000ppm threshold requirement.

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

<sup>(6)</sup> Lead/Ball Finish - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead/Ball Finish values may wrap to two lines if the finish value exceeds the maximum column width.

**Important Information and Disclaimer:** The information provided on this page represents TI's knowledge and belief as of the date that it is provided. TI bases its knowledge and belief on information provided by third parties, and makes no representation or warranty as to the accuracy of such information. Efforts are underway to better integrate information from third parties. TI has taken and continues to take reasonable steps to provide representative and accurate information but may not have conducted destructive testing or chemical analysis on incoming materials and chemicals. TI and TI suppliers consider certain information to be proprietary, and thus CAS numbers and other limited information may not be available for release.

In no event shall TI's liability arising out of such information exceed the total purchase price of the TI part(s) at issue in this document sold by TI to Customer on an annual basis.

**OTHER QUALIFIED VERSIONS OF CC2541 :**

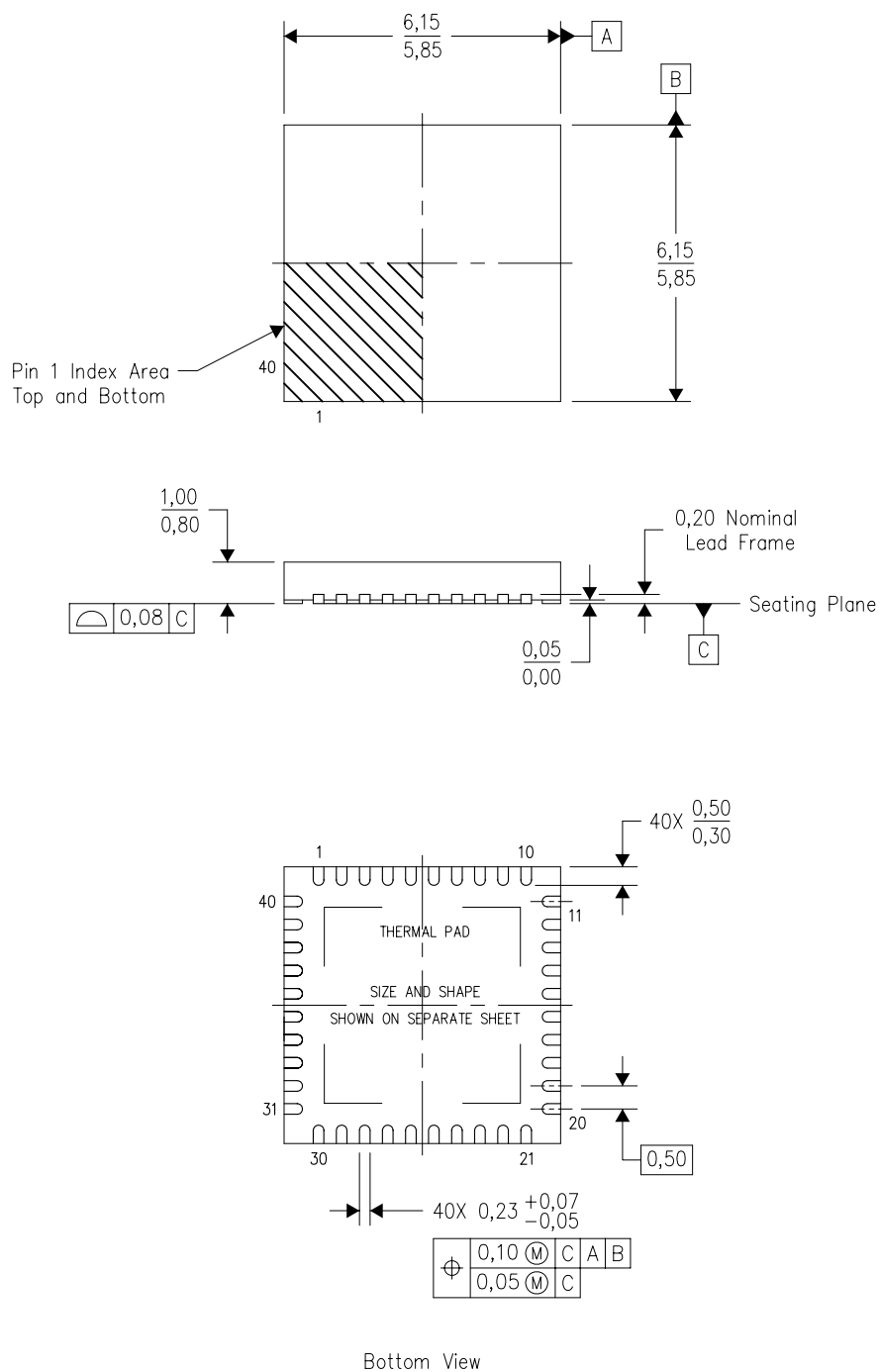
- Automotive: [CC2541-Q1](#)

NOTE: Qualified Version Definitions:

- Automotive - Q100 devices qualified for high-reliability automotive applications targeting zero defects

RHA (S-PVQFN-N40)

PLASTIC QUAD FLATPACK NO-LEAD



4204276/E 06/11

- NOTES:
- All linear dimensions are in millimeters. Dimensioning and tolerancing per ASME Y14.5M-1994.
  - This drawing is subject to change without notice.
  - QFN (Quad Flatpack No-Lead) Package configuration.
  - The package thermal pad must be soldered to the board for thermal and mechanical performance.
  - See the additional figure in the Product Data Sheet for details regarding the exposed thermal pad features and dimensions.
  - Package complies to JEDEC MO-220 variation VJJD-2.

## THERMAL PAD MECHANICAL DATA

RHA (S-PVQFN-N40)

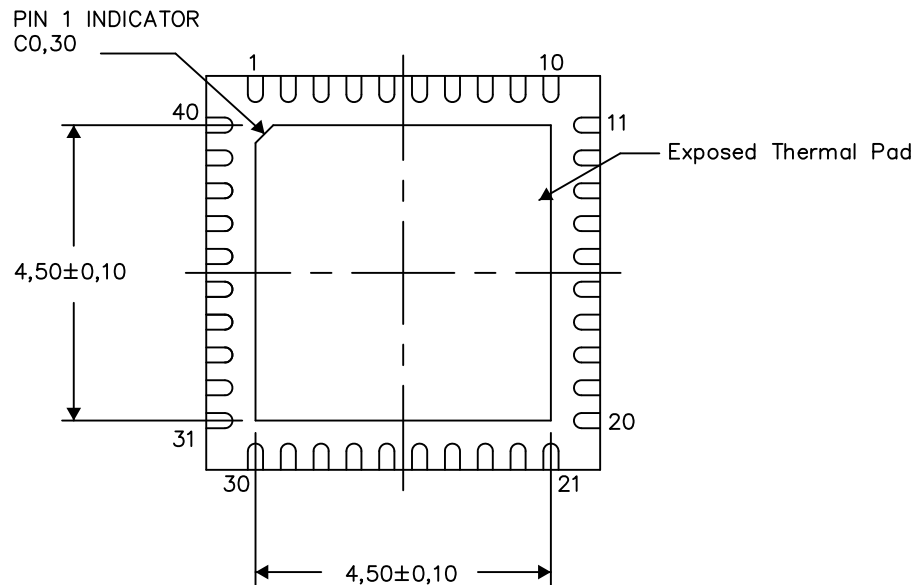
PLASTIC QUAD FLATPACK NO-LEAD

### THERMAL INFORMATION

This package incorporates an exposed thermal pad that is designed to be attached directly to an external heatsink. The thermal pad must be soldered directly to the printed circuit board (PCB). After soldering, the PCB can be used as a heatsink. In addition, through the use of thermal vias, the thermal pad can be attached directly to the appropriate copper plane shown in the electrical schematic for the device, or alternatively, can be attached to a special heatsink structure designed into the PCB. This design optimizes the heat transfer from the integrated circuit (IC).

For information on the Quad Flatpack No-Lead (QFN) package and its advantages, refer to Application Report, QFN/SON PCB Attachment, Texas Instruments Literature No. SLUA271. This document is available at [www.ti.com](http://www.ti.com).

The exposed thermal pad dimensions for this package are shown in the following illustration.

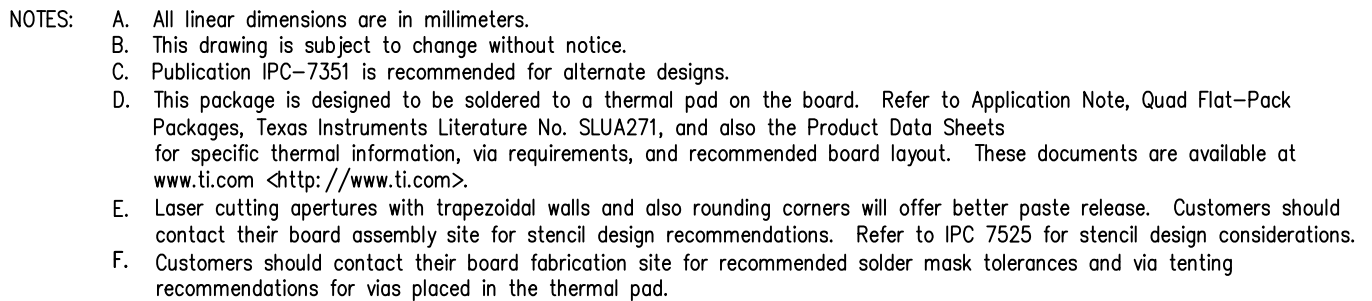


Bottom View

Exposed Thermal Pad Dimensions

4206355-4/X 08/14

NOTES: A. All linear dimensions are in millimeters



## IMPORTANT NOTICE AND DISCLAIMER

TI PROVIDES TECHNICAL AND RELIABILITY DATA (INCLUDING DATASHEETS), DESIGN RESOURCES (INCLUDING REFERENCE DESIGNS), APPLICATION OR OTHER DESIGN ADVICE, WEB TOOLS, SAFETY INFORMATION, AND OTHER RESOURCES "AS IS" AND WITH ALL FAULTS, AND DISCLAIMS ALL WARRANTIES, EXPRESS AND IMPLIED, INCLUDING WITHOUT LIMITATION ANY IMPLIED WARRANTIES OF MERCHANTABILITY, FITNESS FOR A PARTICULAR PURPOSE OR NON-INFRINGEMENT OF THIRD PARTY INTELLECTUAL PROPERTY RIGHTS.

These resources are intended for skilled developers designing with TI products. You are solely responsible for (1) selecting the appropriate TI products for your application, (2) designing, validating and testing your application, and (3) ensuring your application meets applicable standards, and any other safety, security, or other requirements. These resources are subject to change without notice. TI grants you permission to use these resources only for development of an application that uses the TI products described in the resource. Other reproduction and display of these resources is prohibited. No license is granted to any other TI intellectual property right or to any third party intellectual property right. TI disclaims responsibility for, and you will fully indemnify TI and its representatives against, any claims, damages, costs, losses, and liabilities arising out of your use of these resources.

TI's products are provided subject to TI's Terms of Sale ([www.ti.com/legal/termsofsale.html](http://www.ti.com/legal/termsofsale.html)) or other applicable terms available either on [ti.com](http://ti.com) or provided in conjunction with such TI products. TI's provision of these resources does not expand or otherwise alter TI's applicable warranties or warranty disclaimers for TI products.

Mailing Address: Texas Instruments, Post Office Box 655303, Dallas, Texas 75265  
Copyright © 2020, Texas Instruments Incorporated